

# Datasheet

**G32F031x8**

**G32M3122x8**

**G32M3114x8**

**G32M3115x8**

**Arm® Cortex® -M0+ core-based 32-bit MCU**

**Version: V1.3**

# 1 Product Characteristics

## ■ Core

- 32-bit Arm® Cortex®-M0+ core
- Up to 64MHz working frequency

## ■ Memory and interface

- Flash: Up to 64KB
- SRAM: 8KB

## ■ Clock

- HSICLK: Built-in 64MHz high-frequency RC oscillator
- LSICLK: Built-in 32.768KHz low-frequency RC oscillator

## ■ Power and power management

- VDD range: 1.8~5.5V
- Support power-on/power-off (POR/PDR)
- Support programmable voltage detector (PVD)

## ■ Low power mode

- Support sleep, stop and standby modes

## ■ DMA

- 1 DMA with 2 channels

## ■ Debugging interface

- SWD

## ■ I/O

- Up to 29 I/O
- All I/Os can be mapped to external interrupt vectors
- Up to 29 I/O tolerating 5V inputs

## ■ Communication peripherals

- 1 USART, 1 UART support LIN function
- 1 SPI
- 1 I2C

## ■ Analog peripherals

- 1 12-bit ADC, support up to 8+2 external channels and 5 internal channels, with conversion range from 0V~5V. Maximum sampling rate 1.78 MSPS
- 4 programmable analog comparators (COMP)

- 2 rail-to-rail operational amplifiers (OPAMP)

## ■ Timer

- 1 16-bit advanced timer that can provide 8-channel PWM output, support for deadband generation and brake inputs
- 1 32-bit general-purpose timer with 4 independent channels for input capture, output comparison, PWM and pulse counting
- 2 16-bit basic timer
- 1 16-bit low-power timer
- 2 watchdog timers: an independent watchdog IWDG and a window watchdog WWDG
- 1 24-bit self-reducing SysTick Timer

## ■ Integrated driver(only M3114 supported)

- 6N 200V Gate Driver
- 5V LDO, Drive power supply voltage: 5V~20V

## ■ Integrated driver(only M3115 supported)

- 6N 200V Gate Driver
- Drive power supply voltage: 5.5V~20V

## ■ Integrated driver(only M3122 supported)

- 3P3N 40V Gate Driver
- 5V LDO, Drive power supply voltage: 5.5V~30V

## ■ Algorithm unit

- CRC
- DIV

## ■ 96-bit unique device ID

## ■ Chip package

- F031:LQFP32/QFN32/QFN24/QFN20/SSOP28/SSOP24
- M3122:LQFP32/SSOP28/SSOP24
- M3114: LQFP48/QFN40
- M3115:QFN40

# Contents

|          |                                                      |           |
|----------|------------------------------------------------------|-----------|
| <b>1</b> | <b>Product Characteristics .....</b>                 | <b>1</b>  |
| <b>2</b> | <b>Product Information for F031 .....</b>            | <b>6</b>  |
| <b>3</b> | <b>Product Information for M3114/M3115 .....</b>     | <b>7</b>  |
| <b>4</b> | <b>Product Information for M3122.....</b>            | <b>9</b>  |
| <b>5</b> | <b>Pin Information .....</b>                         | <b>11</b> |
| 5.1      | Pin distribution for F031 .....                      | 11        |
| 5.2      | Pin function description for F031 .....              | 13        |
| 5.3      | Pin distribution for M3122/M3114/M3115 .....         | 17        |
| 5.4      | Pin function description for M3122/M3114/M3115 ..... | 20        |
| 5.5      | GPIO multiplexing configuration .....                | 25        |
| <b>6</b> | <b>Functional Description.....</b>                   | <b>30</b> |
| 6.1      | System Architecture .....                            | 30        |
| 6.1.1    | System Block Diagram for F031 .....                  | 30        |
| 6.1.2    | System Block Diagram for M3114.....                  | 31        |
| 6.1.3    | Logic truth value of the drive.....                  | 31        |
| 6.1.1    | System Block Diagram for M3115.....                  | 32        |
| 6.1.2    | Logic truth value of the drive.....                  | 32        |
| 6.1.3    | System Block Diagram for M3122.....                  | 33        |
| 6.1.4    | Logic truth value of the drive.....                  | 33        |
| 6.1.5    | Address Mapping .....                                | 34        |
| 6.1.6    | Start boot mode.....                                 | 35        |
| 6.2      | Core .....                                           | 35        |
| 6.3      | Interrupt controller.....                            | 35        |
| 6.3.1    | Nested Vector Interrupt Controller (NVIC).....       | 35        |
| 6.3.2    | External Interrupt/Event Controller (EINT).....      | 35        |
| 6.4      | On-chip memory .....                                 | 35        |
| 6.5      | Clock .....                                          | 36        |
| 6.5.1    | Clock tree.....                                      | 36        |
| 6.5.2    | Clock sources .....                                  | 36        |

|          |                                                     |           |
|----------|-----------------------------------------------------|-----------|
| 6.5.3    | System clock.....                                   | 36        |
| 6.5.4    | Bus clock .....                                     | 36        |
| 6.6      | Power and power management.....                     | 37        |
| 6.6.1    | Power solution .....                                | 37        |
| 6.6.2    | Voltage regulator .....                             | 37        |
| 6.6.3    | Power supply voltage detector.....                  | 37        |
| 6.7      | Low power mode .....                                | 37        |
| 6.8      | DMA.....                                            | 38        |
| 6.9      | GPIO .....                                          | 38        |
| 6.10     | Communication peripherals.....                      | 38        |
| 6.10.1   | USART/UART .....                                    | 38        |
| 6.10.2   | I2C.....                                            | 39        |
| 6.10.3   | SPI.....                                            | 39        |
| 6.11     | Analog peripherals.....                             | 39        |
| 6.11.1   | ADC.....                                            | 39        |
| 6.11.2   | Comparator (COMP) .....                             | 40        |
| 6.11.3   | Operational amplifier (OPAMP) .....                 | 40        |
| 6.12     | Timer .....                                         | 40        |
| 6.13     | CRC .....                                           | 41        |
| 6.14     | DIV .....                                           | 41        |
| 6.15     | Gate driver .....                                   | 41        |
| 6.15.1   | M3114.....                                          | 41        |
| 6.15.2   | Main characteristics.....                           | 42        |
| 6.15.3   | M3115.....                                          | 42        |
| 6.15.4   | Main characteristics.....                           | 42        |
| 6.15.5   | M3122.....                                          | 43        |
| 6.15.6   | Main characteristics.....                           | 43        |
| <b>7</b> | <b>Electrical Characteristics.....</b>              | <b>44</b> |
| 7.1      | Test Conditions of Electrical Characteristics ..... | 44        |
| 7.1.1    | Maximum and Minimum Values .....                    | 44        |
| 7.1.2    | Typical values .....                                | 44        |
| 7.1.3    | Typical curve .....                                 | 44        |

|        |                                                                      |    |
|--------|----------------------------------------------------------------------|----|
| 7.1.4  | Power Supply Scheme .....                                            | 45 |
| 7.1.5  | Load Capacitance .....                                               | 45 |
| 7.2    | Testing under General Working Conditions .....                       | 46 |
| 7.3    | Absolute Maximum Rating .....                                        | 46 |
| 7.3.1  | Maximum Temperature Characteristics .....                            | 46 |
| 7.3.2  | Maximum Rated Voltage Characteristics .....                          | 46 |
| 7.3.3  | Maximum Rated Current Characteristics .....                          | 47 |
| 7.3.4  | ESD Characteristics .....                                            | 47 |
| 7.3.5  | Latch-up .....                                                       | 47 |
| 7.4    | On-Chip Memory .....                                                 | 47 |
| 7.4.1  | Flash Characteristics .....                                          | 47 |
| 7.5    | Clock System .....                                                   | 48 |
| 7.5.1  | Characteristics of Internal Clock Source .....                       | 48 |
| 7.6    | Power Management .....                                               | 49 |
| 7.6.1  | Power-on/power-down characteristics .....                            | 49 |
| 7.6.2  | Characteristic test of embedded reset and power control module ..... | 49 |
| 7.6.3  | BG .....                                                             | 50 |
| 7.7    | Power Consumption .....                                              | 50 |
| 7.7.1  | Power consumption test environment .....                             | 50 |
| 7.7.2  | Running mode .....                                                   | 51 |
| 7.8    | Wake-up Time in Low Power Mode .....                                 | 52 |
| 7.9    | I/O Port Characteristics .....                                       | 52 |
| 7.10   | NRST pin characteristics .....                                       | 53 |
| 7.11   | Communication Interface .....                                        | 53 |
| 7.11.1 | I2C Interface Characteristics .....                                  | 53 |
| 7.11.2 | SPI Interface Characteristics .....                                  | 55 |
| 7.12   | ADC .....                                                            | 57 |
| 7.12.1 | 12-bit ADC Characteristics .....                                     | 57 |
| 7.12.2 | Temperature Sensor Characteristics .....                             | 59 |
| 7.13   | Comparator .....                                                     | 59 |
| 7.14   | Operational amplifier .....                                          | 59 |
| 7.15   | Gate driver for M3114 .....                                          | 60 |
| 7.15.1 | General Working Conditions .....                                     | 60 |

|                                                            |           |
|------------------------------------------------------------|-----------|
| 7.15.2 Electrical characteristic.....                      | 60        |
| 7.16 Gate driver for M3115 .....                           | 63        |
| 7.16.1 General Working Conditions .....                    | 63        |
| 7.16.2 Electrical characteristic.....                      | 63        |
| 7.17 Gate driver for M3122.....                            | 65        |
| 7.17.1 General Working Conditions .....                    | 65        |
| 7.17.2 Electrical characteristic.....                      | 65        |
| <b>8 Package Information .....</b>                         | <b>67</b> |
| 8.1 LQFP48 Package Information .....                       | 67        |
| 8.2 LQFP32 Package Information .....                       | 67        |
| 8.3 QFN40 Package Information .....                        | 68        |
| 8.4 QFN32 Package Information .....                        | 68        |
| 8.5 QFN24 Package Information .....                        | 69        |
| 8.6 QFN20 Package Information .....                        | 69        |
| 8.7 SSOP28 Package Information.....                        | 70        |
| 8.8 SSOP24 Package Information.....                        | 70        |
| 8.9 Package Designator .....                               | 71        |
| <b>9 Packaging Information .....</b>                       | <b>73</b> |
| 9.1 Tray packaging .....                                   | 73        |
| 9.2 Tube packaging .....                                   | 74        |
| <b>10 Ordering Information.....</b>                        | <b>75</b> |
| <b>11 Commonly Used Function Module Denomination .....</b> | <b>77</b> |
| <b>12 Revision.....</b>                                    | <b>78</b> |

## 2 Product Information for F031

See the following table for product functions and peripheral configuration.

Table 1 Functions and Peripherals

| Product                            |                          | G32F031                                                                                          |                     |                     |                     |        |        |
|------------------------------------|--------------------------|--------------------------------------------------------------------------------------------------|---------------------|---------------------|---------------------|--------|--------|
| Model                              |                          | K8Tx <sup>(1)</sup>                                                                              | K8Ux <sup>(1)</sup> | E8Ux <sup>(1)</sup> | F8Ux <sup>(1)</sup> | G8S6   | E8S6   |
| Package                            |                          | LQFP32                                                                                           | QFN32               | QFN24               | QFN20               | SSOP28 | SSOP24 |
| Core and maximum working frequency |                          | Arm® 32-bit Cortex®-M0+@64MHz                                                                    |                     |                     |                     |        |        |
| Working voltage                    |                          | 1.8~5.5V                                                                                         |                     |                     |                     |        |        |
| Flash (KB)                         |                          | 64                                                                                               |                     |                     |                     |        |        |
| SRAM (KB)                          |                          | 8                                                                                                |                     |                     |                     |        |        |
| DMA                                |                          | 1                                                                                                |                     |                     |                     |        |        |
| GPIOs                              |                          | 29                                                                                               | 23                  | 19                  | 26                  | 22     |        |
| Algorithm units                    | CRC                      | 1                                                                                                |                     |                     |                     |        |        |
|                                    | DIV                      | 1                                                                                                |                     |                     |                     |        |        |
| Timers                             | 16-bit advanced (ATMR)   | 1                                                                                                |                     |                     |                     |        |        |
|                                    | 32-bit general (GTMR)    | 1                                                                                                |                     |                     |                     |        |        |
|                                    | 16-bit basic (BTMR)      | 2                                                                                                |                     |                     |                     |        |        |
|                                    | 24-bit SysTick (SYSTICK) | 1                                                                                                |                     |                     |                     |        |        |
|                                    | Watchdog                 | 2 (IWDG+WWDT)                                                                                    |                     |                     |                     |        |        |
|                                    | LPTMR                    | 1                                                                                                |                     |                     |                     |        |        |
| Communication interfaces           | U(S)ART                  | 1+1                                                                                              |                     |                     |                     |        |        |
|                                    | I2C                      | 1                                                                                                |                     |                     |                     |        |        |
|                                    | SPI                      | 1                                                                                                |                     |                     |                     |        |        |
| 12-bit ADC                         | Unit                     | 1                                                                                                |                     |                     |                     |        |        |
|                                    | External channel         | 8+2                                                                                              | 6+2                 | 3+2                 | 8+2                 | 6+2    |        |
|                                    | Internal channel         | 5                                                                                                |                     |                     |                     |        |        |
| Comparator                         |                          | 4                                                                                                |                     |                     |                     |        |        |
| Operational amplifier (OPAMP)      |                          | 2                                                                                                |                     |                     |                     |        |        |
| Temperature sensor                 |                          | 1                                                                                                |                     |                     |                     |        |        |
| Operating temperature              |                          | Ambient temperature: -40℃ to 85℃/-40℃ to 105℃<br>Junction temperature: -40℃ to 105℃/-40℃ to 125℃ |                     |                     |                     |        |        |

Notes:

- (1) When x is 6, the ambient temperature is -40℃ to 85℃, and the junction temperature is -40℃ to 105℃.  
When x is 7, the ambient temperature is -40℃ to 105℃, and the junction temperature is -40℃ to 125℃.

### 3 Product Information for M3114/M3115

See the following table for product functions and peripheral configuration.

Table 2 Functions and Peripherals

| Product                            |                          | G32M3114                                      |                     | G32M3115            |
|------------------------------------|--------------------------|-----------------------------------------------|---------------------|---------------------|
| Model                              |                          | C8Tx <sup>(1)</sup>                           | H8Ux <sup>(1)</sup> | H8Ux <sup>(1)</sup> |
| Package                            |                          | LQFP48                                        | QFN40               |                     |
| Core and maximum working frequency |                          | Arm® 32-bit Cortex®-M0+@64MHz                 |                     |                     |
| Working voltage                    |                          | 1.8~5.5V                                      |                     |                     |
| Flash (KB)                         |                          | 64                                            |                     |                     |
| SRAM (KB)                          |                          | 8                                             |                     |                     |
| DMA                                |                          | 1                                             |                     |                     |
| GPIOs                              |                          | 23                                            |                     |                     |
| Algorithm units                    | CRC                      | 1                                             |                     |                     |
|                                    | DIV                      | 1                                             |                     |                     |
| Timers                             | 16-bit advanced (ATMR)   | 1                                             |                     |                     |
|                                    | 32-bit general (GTMR)    | 1                                             |                     |                     |
|                                    | 16-bit basic (BTMR)      | 2                                             |                     |                     |
|                                    | 24-bit SysTick (SYSTICK) | 1                                             |                     |                     |
|                                    | Watchdog                 | 2（IWDT+WWDT）                                  |                     |                     |
|                                    | LPTMR                    | 1                                             |                     |                     |
| Communication interfaces           | U(S)ART                  | 1+1                                           |                     |                     |
|                                    | I2C                      | 1                                             |                     |                     |
|                                    | SPI                      | 1                                             |                     |                     |
| 12-bit ADC                         | Unit                     | 1                                             |                     |                     |
|                                    | External channel         | 8+2                                           |                     |                     |
|                                    | Internal channel         | 5                                             |                     |                     |
| Comparator                         |                          | 4                                             |                     |                     |
| Operational amplifier (OPAMP)      |                          | 2                                             |                     |                     |
| Temperature sensor                 |                          | 1                                             |                     |                     |
| Drive power supply voltage         |                          | 5~20V                                         | 5.5~20V             |                     |
| Gate Driver                        |                          | 6N                                            |                     |                     |
| Levitation offset voltage          |                          | 200V                                          |                     |                     |
| Operating temperature              |                          | Ambient temperature: -40℃ to 85℃/-40℃ to 105℃ |                     |                     |

|         |                                                 |          |
|---------|-------------------------------------------------|----------|
| Product | G32M3114                                        | G32M3115 |
|         | Junction temperature: -40℃ to 105℃/-40℃ to 125℃ |          |

**Notes:**

- (1) When x is 6, the ambient temperature is -40℃ to 85℃, and the junction temperature is -40℃ to 105℃.  
When x is 7, the ambient temperature is -40℃ to 105℃, and the junction temperature is -40℃ to 125℃.

## 4 Product Information for M3122

See the following table for product functions and peripheral configuration.

Table 3 Functions and Peripherals

|                                             |                          |                                               |        |        |
|---------------------------------------------|--------------------------|-----------------------------------------------|--------|--------|
| Product                                     |                          | G32M3122                                      |        |        |
| Model                                       |                          | K8Tx <sup>(1)</sup>                           | G8S6   | E8S6   |
| Package                                     |                          | LQFP32                                        | SSOP28 | SSOP24 |
| Core and maximum working frequency          |                          | Arm® 32-bit Cortex®-M0+@64MHz                 |        |        |
| Working voltage                             |                          | 1.8~5.5V                                      |        |        |
| Flash (KB)                                  |                          | 64                                            |        |        |
| SRAM (KB)                                   |                          | 8                                             |        |        |
| DMA                                         |                          | 1                                             |        |        |
| GPIOs                                       |                          | 22                                            | 19     | 15     |
| Algorithm units                             | CRC                      | 1                                             |        |        |
|                                             | DIV                      | 1                                             |        |        |
| Timers                                      | 16-bit advanced (ATMR)   | 1                                             |        |        |
|                                             | 32-bit general (GTMR)    | 1                                             |        |        |
|                                             | 16-bit basic (BTMR)      | 2                                             |        |        |
|                                             | 24-bit SysTick (SYSTICK) | 1                                             |        |        |
|                                             | Watchdog                 | 2 (IWDG+WWDT)                                 |        |        |
|                                             | LPTMR                    | 1                                             |        |        |
| Communication interfaces                    | U(S)ART                  | 1+1                                           |        |        |
|                                             | I2C                      | 1                                             |        |        |
|                                             | SPI                      | 1                                             |        |        |
| 12-bit ADC                                  | Unit                     | 1                                             |        |        |
|                                             | External channel         | 8+2                                           |        | 6+2    |
|                                             | Internal channel         | 5                                             |        |        |
| Comparator                                  |                          | 4                                             |        |        |
| Operational amplifier (OPAMP)               |                          | 2                                             |        |        |
| Temperature sensor                          |                          | 1                                             |        |        |
| Supply voltage of the built-in driver.      |                          | 5.5~30V                                       |        |        |
| Gate Driver                                 |                          | 3P3N                                          |        |        |
| Withstand voltage of the drive power supply |                          | 40V                                           |        |        |
| Operating temperature                       |                          | Ambient temperature: -40℃ to 85℃/-40℃ to 105℃ |        |        |

|         |                                                 |
|---------|-------------------------------------------------|
| Product | G32M3122                                        |
|         | Junction temperature: -40℃ to 105℃/-40℃ to 125℃ |

Notes:

- (1) When x is 6, the ambient temperature is -40℃ to 85℃, and the junction temperature is -40℃ to 105℃.
- (2) When x is 7, the ambient temperature is -40℃ to 105℃, and the junction temperature is -40℃ to 125℃.

## 5 Pin Information

### 5.1 Pin distribution for F031

Figure 1 LQFP32 Pin Distribution Diagram

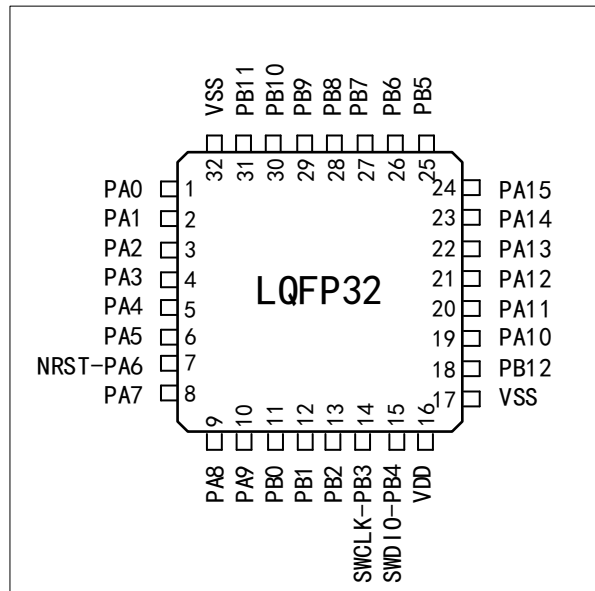


Figure 2 QFN32 Pin Distribution Diagram

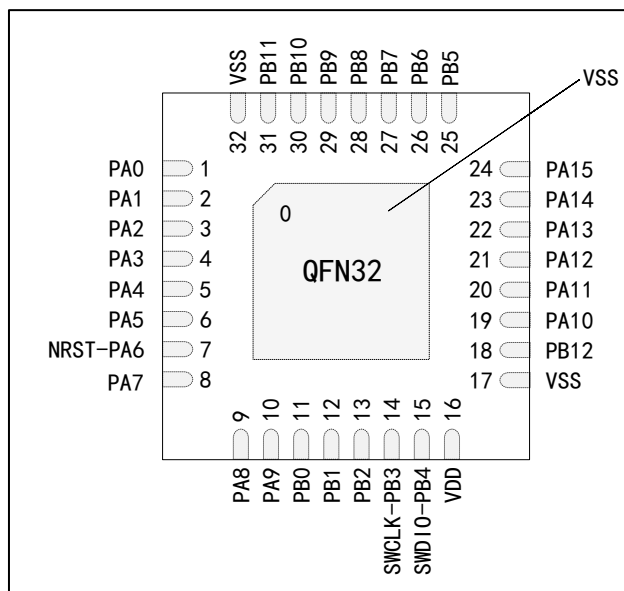


Figure 3 QFN24 Pin Distribution Diagram

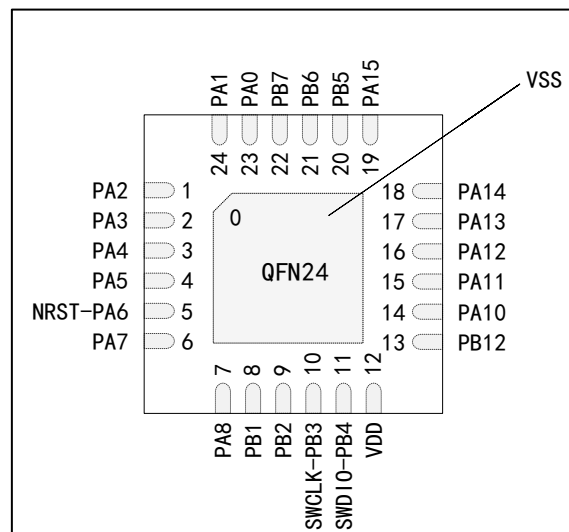


Figure 4 QFN20 Pin Distribution Diagram

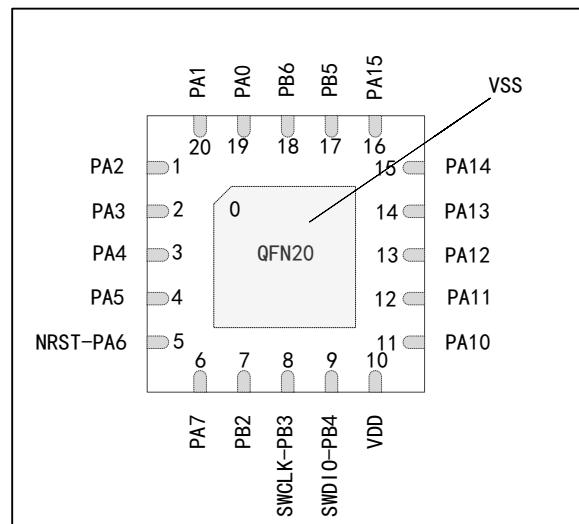


Figure 5 SSOP28 Pin Distribution Diagram

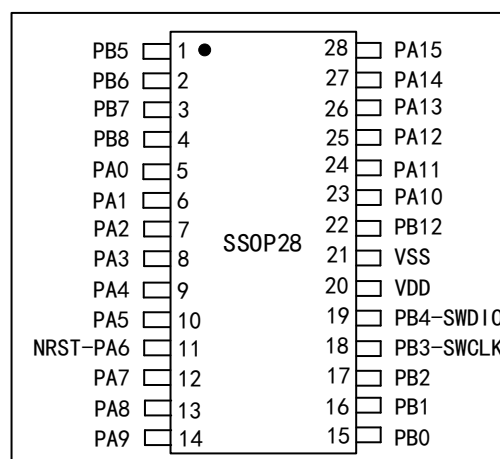
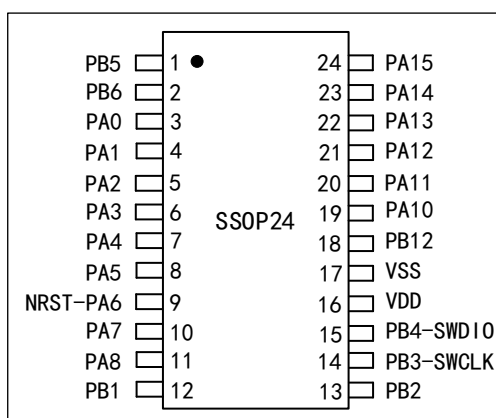


Figure 6 SSOP24 Pin Distribution Diagram



## 5.2 Pin function description for F031

Table 4 Legends/Abbreviations Used in Output Pin Table

| Name          |                               | Abbreviation                                                                                                                               | Definition                                       |
|---------------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------|
| Pin name      |                               | Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name |                                                  |
| Pin type      |                               | P                                                                                                                                          | Power pin                                        |
|               |                               | I                                                                                                                                          | Only input pin                                   |
|               |                               | O                                                                                                                                          | Only output pin                                  |
|               |                               | I/O                                                                                                                                        | I/O pin                                          |
| I/O structure |                               | 5T                                                                                                                                         | 5V tolerant FT I/O                               |
|               |                               | STDA                                                                                                                                       | 3.3V standard I/O, directly connected to ADC     |
|               |                               | STD                                                                                                                                        | 3.3V standard I/O                                |
|               |                               | B                                                                                                                                          | Dedicated Boot0 pin                              |
|               |                               | RST                                                                                                                                        | One-way reset pin with built-in pull-up resistor |
| Notes         |                               | Unless otherwise specified in the notes, all I/O is set as floating input during and after reset                                           |                                                  |
| Pin function  | Default multiplexing function | Select this function through AFIO remapping registers                                                                                      |                                                  |
|               | Additional function           | Select this function directly through peripheral registers                                                                                 |                                                  |

Table 5 Descriptions by Pin Number

| LQFP32 /QFN32 | QFN24 | QFN20 | SSOP28 | SSOP24 | Pin Name (After reset) | Digital Multiplexing Function | Analog Multiplexing Function | Type               |
|---------------|-------|-------|--------|--------|------------------------|-------------------------------|------------------------------|--------------------|
| 1             | 23    | 19    | 5      | 3      | PA0                    | USART_TX<br>SPI_CS<br>I2C_SCL | OPAMP0_OUT<br>COMP3_INN      | I/O <sup>(1)</sup> |

| LQFP32<br>/QFN32 | QFN24 | QFN20 | SSOP28 | SSOP24 | Pin Name<br>(After<br>reset) | Digital<br>Multiplexing<br>Function                                     | Analog<br>Multiplexing<br>Function | Type |
|------------------|-------|-------|--------|--------|------------------------------|-------------------------------------------------------------------------|------------------------------------|------|
| 2                | 24    | 20    | 6      | 4      | PA1                          | USART_RX<br>SPI_SCK<br>I2C_SDA                                          | OPAMP0_INN<br>COMP1_INN            | I/O  |
| 3                | 1     | 1     | 7      | 5      | PA2                          | USART_CTS<br>SPI_MOSI                                                   | OPAMP0_INP<br>COMP2_INN            | I/O  |
| 4                | 2     | 2     | 8      | 6      | PA3                          | USART_RTS<br>SPI_MISO                                                   | OPAMP1_INP                         | I/O  |
| 5                | 3     | 3     | 9      | 7      | PA4                          | USART_CK                                                                | OPAMP1_INN                         | I/O  |
| 6                | 4     | 4     | 10     | 8      | PA5                          | ATMR_BKIN<br>COMP0_OUT                                                  | OPAMP1_OUT                         | I/O  |
| 7                | 5     | 5     | 11     | 9      | NRST<br>(PA6)                | NRST                                                                    | -                                  | I/O  |
| 8                | 6     | 6     | 12     | 10     | PA7                          | UART_TX<br>I2C_SCL<br>ATMR_BKIN<br>GTMR_CH0_ETR<br>BTMR1_CH0<br>WAKEUP0 | ADC_IN0<br>COMP0_INP               | I/O  |
| 9                | 7     | -     | 13     | 11     | PA8                          | UART_RX<br>I2C_SDA<br>ATMR_ETR<br>GTMR_CH1<br>BTMR1_CH0<br>CLKOUT       | ADC_IN1<br>COMP0_INN0              | I/O  |
| 10               | -     | -     | 14     | -      | PA9                          | I2C_SMBA<br>ATMR_CH3<br>GTMR_CH2<br>COMP1_OUT                           | ADC_IN2<br>COMP0_INN1              | I/O  |
| 11               | -     | -     | 15     | -      | PB0                          | ATMR_CH3N<br>GTMR_CH3<br>BTMR0_CH0<br>COMP1_OUT                         | ADC_IN3                            | I/O  |
| 12               | 8     | -     | 16     | 12     | PB1                          | UART_TX<br>I2C_SDA<br>ATMR_BKIN<br>GTMR_CH0_ETR<br>COMP0_OUT            | ADC_IN4<br>COMP1_INN<br>VREF+      | I/O  |
| 13               | 9     | 7     | 17     | 13     | PB2                          | UART_RX<br>I2C_SCL<br>ATMR_ETR<br>GTMR_CH1                              | COMP2_INN                          | I/O  |

| LQFP32<br>/QFN32 | QFN24 | QFN20 | SSOP28 | SSOP24 | Pin Name<br>(After<br>reset) | Digital<br>Multiplexing<br>Function                                     | Analog<br>Multiplexing<br>Function | Type |
|------------------|-------|-------|--------|--------|------------------------------|-------------------------------------------------------------------------|------------------------------------|------|
|                  |       |       |        |        |                              | WAKEUP1                                                                 |                                    |      |
| 14               | 10    | 8     | 18     | 14     | SWCLK<br>(PB3)               | SWCLK<br>UART_TX<br>ATMR_CH3N<br>GTMR_CH2<br>BTMR0_CH0                  | -                                  | I/O  |
| 15               | 11    | 9     | 19     | 15     | SWDIO<br>(PB4)               | SWDIO<br>UART_RX<br>ATMR_CH3<br>GTMR_CH3<br>BTMR1_CH0                   | -                                  | I/O  |
| 16               | 12    | 10    | 20     | 16     | VDD                          | Digital power                                                           | -                                  | P    |
| 17               | 0     | 0     | 21     | 17     | VSS                          | Chip ground                                                             | -                                  | P    |
| 18               | 13    | -     | 22     | 18     | PB12                         | USART_RTS<br>SPI_MOSI<br>ATMR_CH3<br>GTMR_CH2<br>BTMR1_CH0<br>COMP2_OUT | ADC_IN5                            | I/O  |
| 19               | 14    | 11    | 23     | 19     | PA10                         | USART_TX<br>ATMR_CH2N <sup>(2)</sup>                                    | -                                  | I/O  |
| 20               | 15    | 12    | 24     | 20     | PA11                         | USART_RX<br>ATMR_CH2 <sup>(2)</sup>                                     | -                                  | I/O  |
| 21               | 16    | 13    | 25     | 21     | PA12                         | USART_CTS<br>SPI_CS<br>ATMR_CH1N <sup>(2)</sup>                         | -                                  | I/O  |
| 22               | 17    | 14    | 26     | 22     | PA13                         | USART_RTS<br>SPI_SCK<br>ATMR_CH1 <sup>(2)</sup>                         | -                                  | I/O  |
| 23               | 18    | 15    | 27     | 23     | PA14                         | USART_CK<br>SPI_MOSI<br>ATMR_CH0N <sup>(2)</sup>                        | -                                  | I/O  |
| 24               | 19    | 16    | 28     | 24     | PA15                         | SPI_MISO<br>ATMR_CH0 <sup>(2)</sup><br>BTMR1_CH0                        | -                                  | I/O  |
| 25               | 20    | 17    | 1      | 1      | PB5                          | UART_TX<br>SPI_CS<br>GTMR_CH2<br>COMP2_OUT                              | ADC_IN6<br>COMP3_INN               | I/O  |
| 26               | 21    | 18    | 2      | 2      | PB6                          | UART_RX<br>SPI_SCK                                                      | ADC_IN7<br>COMP123_INP             | I/O  |

| LQFP32<br>/QFN32 | QFN24 | QFN20 | SSOP28 | SSOP24 | Pin Name<br>(After<br>reset) | Digital<br>Multiplexing<br>Function                                      | Analog<br>Multiplexing<br>Function | Type |
|------------------|-------|-------|--------|--------|------------------------------|--------------------------------------------------------------------------|------------------------------------|------|
|                  |       |       |        |        |                              | I2C_SMBA<br>GTMR_CH3                                                     |                                    |      |
| 27               | 22    | -     | 3      | -      | PB7                          | UART_TX<br>SPI_MISO<br>I2C_SCL<br>GTMR_CH1<br>BTMR0_CH0<br>COMP1_OUT     | -                                  | I/O  |
| 28               | -     | -     | 4      | -      | PB8                          | UART_RX<br>SPI_MOSI<br>I2C_SDA<br>GTMR_CH0_ETR<br>BTMR1_CH0              | -                                  | I/O  |
| 29               | -     | -     | -      | -      | PB9                          | USART_TX<br>SPI_CS<br>ATMR_BKIN<br>GTMR_CH3<br>COMP2_OUT                 | COMP0_INP                          | I/O  |
| 30               | -     | -     | -      | -      | PB10                         | USART_RX<br>SPI_SCK<br>ATMR_ETR<br>GTMR_CH0_ETR<br>COMP0_OUT             | -                                  | I/O  |
| 31               | -     | -     | -      | -      | PB11                         | USART_CTS<br>SPI_MISO<br>ATMR_CH3N<br>GTMR_CH1<br>BTMR0_CH0<br>COMP1_OUT | -                                  | I/O  |
| 32               | 0     | 0     | -      | -      | VSS                          | Chip ground                                                              | -                                  | P    |

### 5.3 Pin distribution for M3122/M3114/M3115

Figure 7 Pin Distribution Diagram of LQFP48 for the M3114 Series

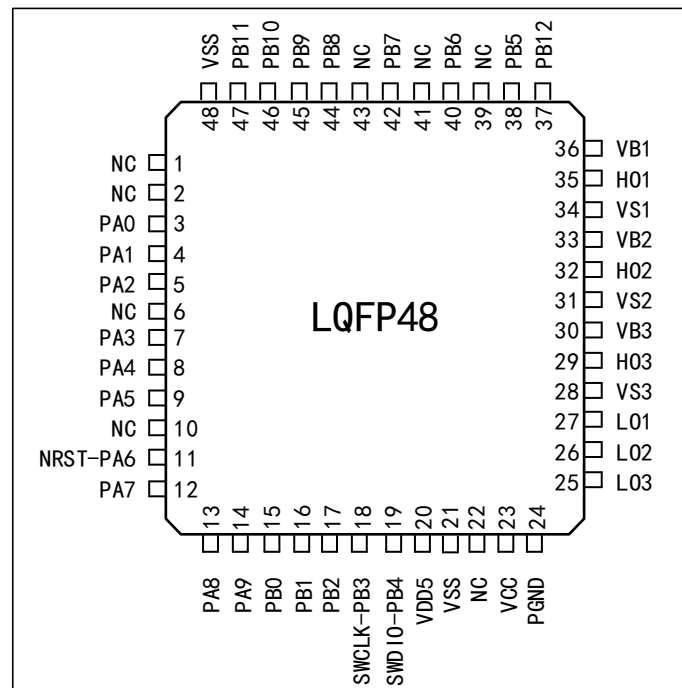


Figure 8 Pin Distribution Diagram of QFN40 for the M3114 Series

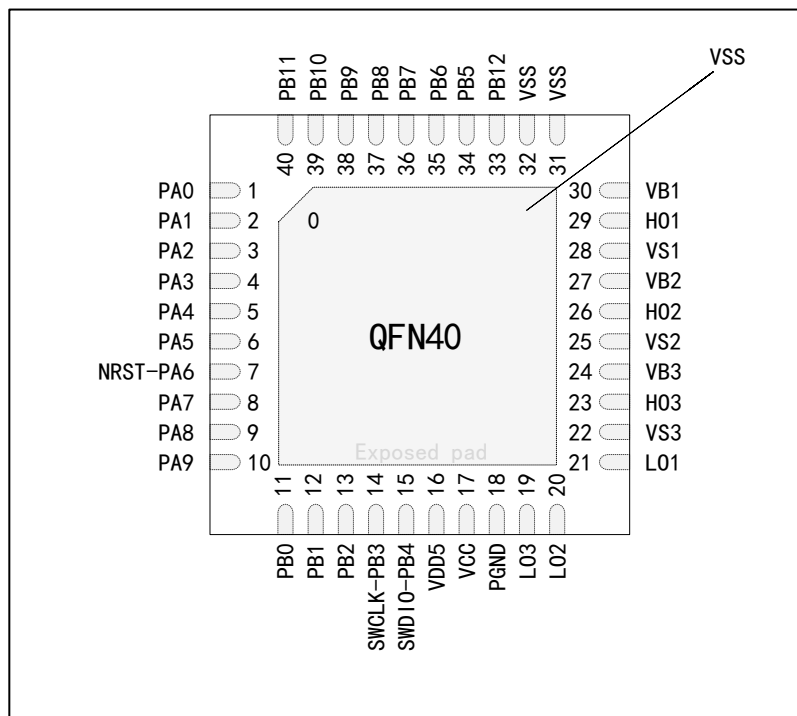


Figure 9 Pin Distribution Diagram of QFN40 for the M3115 Series

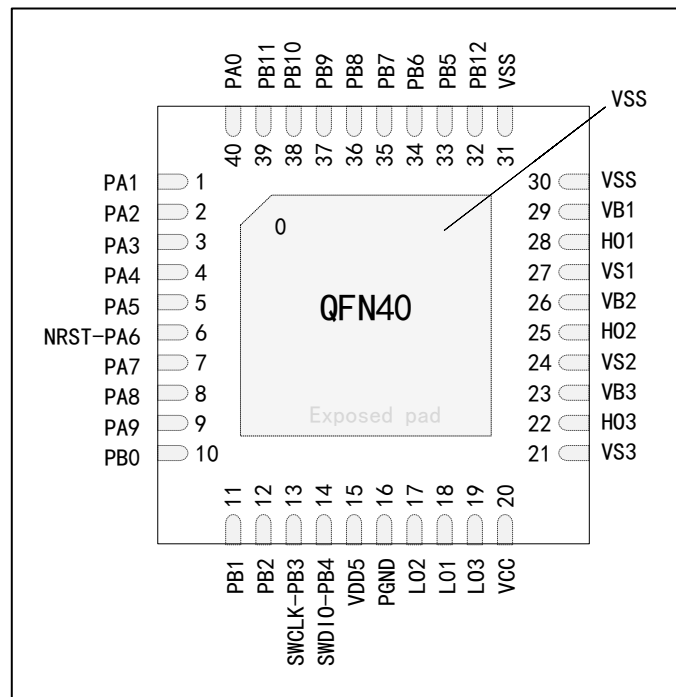


Figure 10 Pin Distribution Diagram of LQFP32 for the M3122 Series

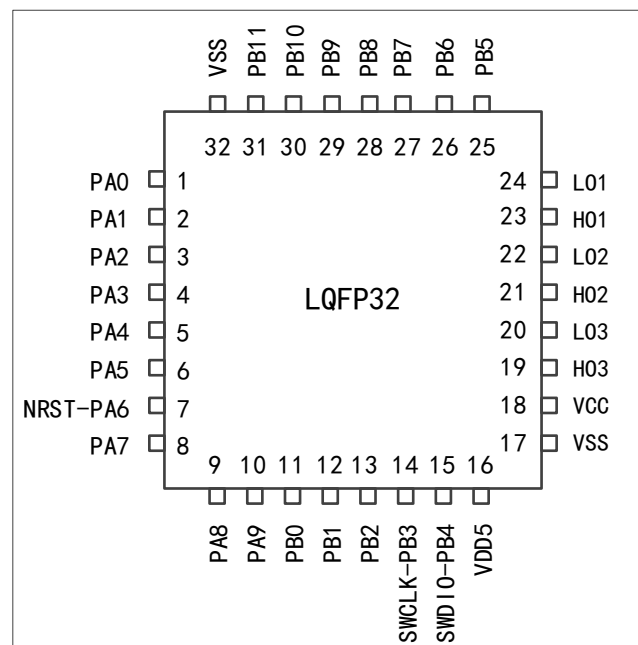


Figure 11 Pin Distribution Diagram of SSOP28 for the M3122 Series

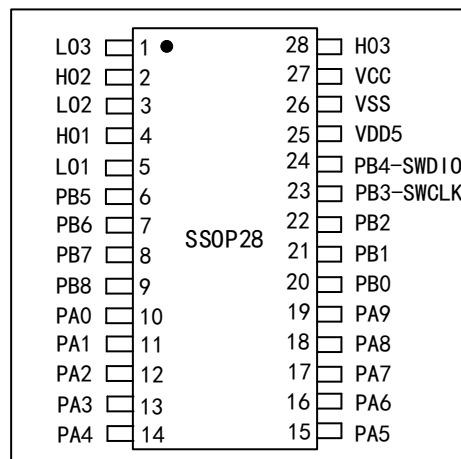
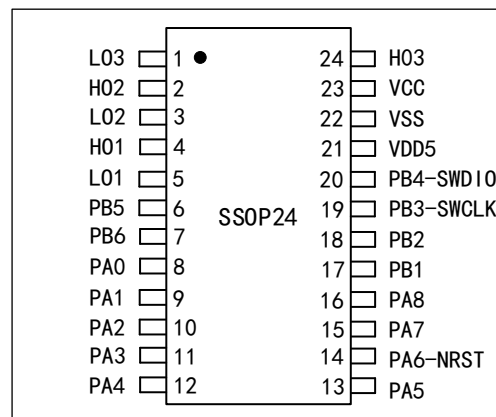


Figure 12 Pin Distribution Diagram of SSOP24 for the M3122 Series



## 5.4 Pin function description for M3122/M3114/M3115

Table 6 Legends/Abbreviations Used in Output Pin Table

| Name          |                               | Abbreviation                                                                                                                               | Definition                                       |
|---------------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------|
| Pin name      |                               | Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name |                                                  |
| Pin type      |                               | P                                                                                                                                          | Power pin                                        |
|               |                               | I                                                                                                                                          | Only input pin                                   |
|               |                               | O                                                                                                                                          | Only output pin                                  |
|               |                               | I/O                                                                                                                                        | I/O pin                                          |
| I/O structure |                               | 5T                                                                                                                                         | 5V tolerant FT I/O                               |
|               |                               | STDA                                                                                                                                       | 3.3V standard I/O, directly connected to ADC     |
|               |                               | STD                                                                                                                                        | 3.3V standard I/O                                |
|               |                               | B                                                                                                                                          | Dedicated Boot0 pin                              |
|               |                               | RST                                                                                                                                        | One-way reset pin with built-in pull-up resistor |
| Notes         |                               | Unless otherwise specified in the notes, all I/O is set as floating input during and after reset                                           |                                                  |
| Pin function  | Default multiplexing function | Select this function through AFIO remapping registers                                                                                      |                                                  |
|               | Additional function           | Select this function directly through peripheral registers                                                                                 |                                                  |

Table 7 Descriptions by Pin Number

| LQFP48 | QFN40(M3114) | QFN40(M3115) | LQFP32 | SSOP28 | SSOP24 | Pin Name<br>(After reset) | Digital<br>Multiplexing Function | Analog<br>Multiplexing Function | Type |
|--------|--------------|--------------|--------|--------|--------|---------------------------|----------------------------------|---------------------------------|------|
| 3      | 1            | 40           | 1      | 10     | 8      | PA0                       | USART_TX<br>SPI_CS<br>I2C_SCL    | OPAMP0_OUT<br>COMP3_INN         | I/O  |

| LQFP48 | QFN40(M3114) | QFN40(M3115) | LQFP32 | SSOP28 | SSOP24 | Pin Name<br>(After reset) | Digital<br>Multiplexing Function                                        | Analog<br>Multiplexing Function | Type |
|--------|--------------|--------------|--------|--------|--------|---------------------------|-------------------------------------------------------------------------|---------------------------------|------|
| 1      | -            | -            | -      | -      | -      | NC                        | -                                                                       | -                               | -    |
| 4      | 2            | 1            | 2      | 11     | 9      | PA1                       | USART_RX<br>SPI_SCK<br>I2C_SDA                                          | OPAMP0_INN<br>COMP1_INN         | I/O  |
| 2      | -            | -            | -      | -      | -      | NC                        | -                                                                       | -                               | -    |
| 5      | 3            | 2            | 3      | 12     | 10     | PA2                       | USART_CTS<br>SPI_MOSI                                                   | OPAMP0_INP<br>COMP2_INN         | I/O  |
| 6      | -            | -            | -      | -      | -      | NC                        | -                                                                       | -                               | -    |
| 7      | 4            | 3            | 4      | 13     | 11     | PA3                       | USART_RTS<br>SPI_MISO                                                   | OPAMP1_INP                      | I/O  |
| 10     | -            | -            | -      | -      | -      | NC                        | -                                                                       | -                               | -    |
| 8      | 5            | 4            | 5      | 14     | 12     | PA4                       | USART_CK                                                                | OPAMP1_INN                      | I/O  |
| 9      | 6            | 5            | 6      | 15     | 13     | PA5                       | ATMR_BKIN<br>COMP0_OUT                                                  | OPAMP1_OUT                      | I/O  |
| 11     | 7            | 6            | 7      | 16     | 14     | NRST (PA6)                | NRST                                                                    | -                               | I/O  |
| 12     | 8            | 7            | 8      | 17     | 15     | PA7                       | UART_TX<br>I2C_SCL<br>ATMR_BKIN<br>GTMR_CH0_ETR<br>BTMR1_CH0<br>WAKEUP0 | ADC_IN0<br>COMP0_INP            | I/O  |
| 13     | 9            | 8            | 9      | 18     | 16     | PA8                       | UART_RX<br>I2C_SDA<br>ATMR_ETR<br>GTMR_CH1<br>BTMR1_CH0<br>CLKOUT       | ADC_IN1<br>COMP0_INN0           | I/O  |

| LQFP48 | QFN40(M3114) | QFN40(M3115) | LQFP32 | SSOP28 | SSOP24 | Pin Name<br>(After reset) | Digital<br>Multiplexing Function                             | Analog<br>Multiplexing Function | Type |
|--------|--------------|--------------|--------|--------|--------|---------------------------|--------------------------------------------------------------|---------------------------------|------|
| 14     | 10           | 9            | 10     | 19     | -      | PA9                       | I2C_SMBA<br>ATMR_CH3<br>GTMR_CH2<br>COMP1_OUT                | ADC_IN2<br>COMP0_INN1           | I/O  |
| 15     | 11           | 10           | 11     | 20     | -      | PB0                       | ATMR_CH3N<br>GTMR_CH3<br>BTMR0_CH0<br>COMP1_OUT              | ADC_IN3                         | I/O  |
| 16     | 12           | 11           | 12     | 21     | 17     | PB1                       | UART_TX<br>I2C_SDA<br>ATMR_BKIN<br>GTMR_CH0_ETR<br>COMP0_OUT | ADC_IN4<br>COMP1_INN<br>VREF+   | I/O  |
| 17     | 13           | 12           | 13     | 22     | 18     | PB2                       | UART_RX<br>I2C_SCL<br>ATMR_ETR<br>GTMR_CH1<br>WAKEUP1        | COMP2_INN                       | I/O  |
| 18     | 14           | 13           | 14     | 23     | 19     | SWCLK (PB3)               | SWCLK<br>UART_TX<br>ATMR_CH3N<br>GTMR_CH2<br>BTMR0_CH0       | -                               | I/O  |
| 19     | 15           | 14           | 15     | 24     | 20     | SWDIO (PB4)               | SWDIO<br>UART_RX<br>ATMR_CH3<br>GTMR_CH3                     | -                               | I/O  |

| LQFP48 | QFN40(M3114) | QFN40(M3115) | LQFP32 | SSOP28 | SSOP24 | Pin Name<br>(After reset) | Digital<br>Multiplexing Function                                        | Analog<br>Multiplexing Function | Type |
|--------|--------------|--------------|--------|--------|--------|---------------------------|-------------------------------------------------------------------------|---------------------------------|------|
|        |              |              |        |        |        |                           | BTMR1_CH0                                                               |                                 |      |
| 20     | 16           | 15           | 16     | 25     | 21     | VDD5                      | Supply voltage                                                          | -                               | P    |
| -      | -            | -            | -      | -      | -      | VDD                       | Digital power                                                           | -                               | P    |
| 21     | 31           | 30           | 17     | 26     | 22     | VSS                       | Chip ground                                                             | -                               | P    |
| 22     | -            | -            | -      | -      | -      | NC                        | -                                                                       | -                               | -    |
| 23     | 17           | 20           | 18     | 27     | 23     | VCC                       | High-voltage supply voltage                                             | -                               | P    |
| 24     | 18           | 16           | -      | -      | -      | PGND                      | High voltage ground                                                     | -                               | P    |
| 25     | 19           | 19           | 20     | 1      | 1      | LO3                       | Low-side output                                                         | -                               | O    |
| 26     | 20           | 17           | 22     | 3      | 3      | LO2                       | Low-side output                                                         | -                               | O    |
| 27     | 21           | 18           | 24     | 5      | 5      | LO1                       | Low-side output                                                         | -                               | O    |
| 28     | 22           | 21           | -      | -      | -      | VS3                       | High-side floating pin                                                  | -                               | P    |
| 29     | 23           | 22           | 19     | 28     | 24     | HO3                       | High-side output                                                        | -                               | O    |
| 30     | 24           | 23           | -      | -      | -      | VB3                       | High-side bootstrap power pin                                           | -                               | P    |
| 31     | 25           | 24           | -      | -      | -      | VS2                       | High-side floating pin                                                  | -                               | P    |
| 32     | 26           | 25           | 21     | 2      | 2      | HO2                       | High-side output                                                        | -                               | O    |
| 33     | 27           | 26           | -      | -      | -      | VB2                       | High-side bootstrap power pin                                           | -                               | P    |
| 34     | 28           | 27           | -      | -      | -      | VS1                       | High-side floating pin                                                  | -                               | P    |
| 35     | 29           | 28           | 23     | 4      | 4      | HO1                       | High-side output                                                        | -                               | O    |
| 36     | 30           | 29           | -      | -      | -      | VB1                       | High-side bootstrap power pin                                           | -                               | P    |
| 37     | 33           | 32           | -      | -      | -      | PB12                      | USART_RTS<br>SPI_MOSI<br>ATMR_CH3<br>GTMR_CH2<br>BTMR1_CH0<br>COMP2_OUT | ADC_IN5                         | I/O  |
| 38     | 34           | 33           | 25     | 6      | 6      | PB5                       | UART_TX<br>SPI_CS                                                       | ADC_IN6<br>COMP3_INN            | I/O  |

| LQFP48 | QFN40(M3114) | QFN40(M3115) | LQFP32 | SSOP28 | SSOP24 | Pin Name<br>(After reset) | Digital<br>Multiplexing Function                                     | Analog<br>Multiplexing Function | Type |
|--------|--------------|--------------|--------|--------|--------|---------------------------|----------------------------------------------------------------------|---------------------------------|------|
|        |              |              |        |        |        |                           | GTMR_CH2<br>COMP2_OUT                                                |                                 |      |
| 39     | -            | -            | -      | -      | -      | NC                        | -                                                                    | -                               | -    |
| 40     | 35           | 34           | 26     | 7      | 7      | PB6                       | UART_RX<br>SPI_SCK<br>I2C_SMBA<br>GTMR_CH3<br>COMP3_OUT              | ADC_IN7<br>COMP123_INP          | I/O  |
| 41     | -            | -            | -      | -      | -      | NC                        | -                                                                    | -                               | -    |
| 42     | 36           | 35           | 27     | 8      | -      | PB7                       | UART_TX<br>SPI_MISO<br>I2C_SCL<br>GTMR_CH1<br>BTMR0_CH0<br>COMP1_OUT | -                               | I/O  |
| 43     | -            | -            | -      | -      | -      | NC                        | -                                                                    | -                               | -    |
| 44     | 37           | 36           | 28     | 9      | -      | PB8                       | UART_RX<br>SPI_MOSI<br>I2C_SDA<br>GTMR_CH0_ETR<br>BTMR1_CH0          | -                               | I/O  |
| 45     | 38           | 37           | 29     | -      | -      | PB9                       | USART_TX<br>SPI_CS<br>ATMR_BKIN<br>GTMR_CH3<br>COMP2_OUT             | COMP0_INP                       | I/O  |
| 46     | 39           | 38           | 30     | -      | -      | PB10                      | USART_RX                                                             | -                               | I/O  |

| LQFP48 | QFN40(M3114) | QFN40(M3115) | LQFP32 | SSOP28 | SSOP24 | Pin Name<br>(After reset) | Digital<br>Multiplexing Function                                         | Analog<br>Multiplexing Function | Type |
|--------|--------------|--------------|--------|--------|--------|---------------------------|--------------------------------------------------------------------------|---------------------------------|------|
|        |              |              |        |        |        |                           | SPI_SCK<br>ATMR_ETR<br>GTMR_CH0_ETR<br>COMP0_OUT                         |                                 |      |
| 47     | 40           | 39           | 31     | -      | -      | PB11                      | USART_CTS<br>SPI_MISO<br>ATMR_CH3N<br>GTMR_CH1<br>BTMR0_CH0<br>COMP1_OUT | -                               | I/O  |
| 48     | 32           | 31           | 32     | 26     | 22     | VSS                       | Chip ground                                                              | -                               | P    |

## 5.5 GPIO multiplexing configuration

Table 8 Multiplexing configuration for port A

|     | AF0       | AF1      | AF2     | AF3       | AF4 | AF5 | AF6 | AF7       | Secondary<br>function | Analog                  |
|-----|-----------|----------|---------|-----------|-----|-----|-----|-----------|-----------------------|-------------------------|
| PA0 | USART_TX  | SPI_CS   | I2C_SCL | -         | -   | -   | -   | -         | -                     | OPAMP0_OUT<br>COMP3_INN |
| PA1 | USART_RX  | SPI_SCK  | I2C_SDA | -         | -   | -   | -   | -         | -                     | OPAMP0_INN<br>COMP1_INN |
| PA2 | USART_CTS | SPI_MOSI | -       | -         | -   | -   | -   | -         | -                     | OPAMP0_INP<br>COMP2_INN |
| PA3 | USART_RTS | SPI_MISO | -       | -         | -   | -   | -   | -         | -                     | OPAMP1_INP              |
| PA4 | USART_CK  | -        | -       | -         | -   | -   | -   | -         | -                     | OPAMP1_INN              |
| PA5 | -         | -        | -       | ATMR_BKIN | -   | -   | -   | COMP0_OUT | -                     | OPAMP1_OUT              |

|      | AF0           | AF1      | AF2      | AF3                      | AF4          | AF5       | AF6 | AF7       | Secondary function | Analog                |
|------|---------------|----------|----------|--------------------------|--------------|-----------|-----|-----------|--------------------|-----------------------|
| PA6  | NRST(Default) | -        | -        | -                        | -            | -         | -   | -         | -                  | -                     |
| PA7  | UART_TX       | -        | I2C_SCL  | ATMR_BKIN                | GTMR_CH0_ETR | BTMR1_CH0 | -   | -         | WAKEUP0            | ADC_IN0<br>COMP0_INP  |
| PA8  | UART_RX       | -        | I2C_SDA  | ATMR_ETR                 | GTMR_CH1     | BTMR1_CH0 | -   | CLKOUT    | -                  | ADC_IN1<br>COMP0_INN0 |
| PA9  | -             | -        | I2C_SMBA | ATMR_CH3                 | GTMR_CH2     | -         | -   | COMP1_OUT |                    | ADC_IN2<br>COMP0_INN1 |
| PA10 | USART_TX      | -        | -        | ATMR_CH2N <sup>(2)</sup> | -            | -         | -   | -         | -                  | -                     |
| PA11 | USART_RX      | -        | -        | ATMR_CH2 <sup>(2)</sup>  | -            | -         | -   | -         | -                  | -                     |
| PA12 | USART_CTS     | SPI_CS   | -        | ATMR_CH1N <sup>(2)</sup> | -            | -         | -   | -         | -                  | -                     |
| PA13 | USART_RTS     | SPI_SCK  | -        | ATMR_CH1 <sup>(2)</sup>  | -            | -         | -   | -         | -                  | -                     |
| PA14 | USART_CK      | SPI_MOSI | -        | ATMR_CH0N <sup>(2)</sup> | -            | -         | -   | -         | -                  | -                     |
| PA15 | -             | SPI_MISO | -        | ATMR_CH0 <sup>(2)</sup>  | -            | BTMR1_CH0 | -   | -         | -                  | -                     |

Table 9 Multiplexing configuration for port B

|     | AF0        | AF1     | AF2     | AF3       | AF4          | AF5       | AF6 | AF7       | Secondary function | Analog                        |
|-----|------------|---------|---------|-----------|--------------|-----------|-----|-----------|--------------------|-------------------------------|
| PB0 | -          | -       | -       | ATMR_CH3N | GTMR_CH3     | BTMR0_CH0 | -   | COMP1_OUT | -                  | ADC_IN3                       |
| PB1 | UART_TX    | -       | I2C_SDA | ATMR_BKIN | GTMR_CH0_ETR | -         | -   | COMP0_OUT | -                  | ADC_IN4<br>COMP1_INN<br>VREF+ |
| PB2 | UART_RX    | -       | I2C_SCL | ATMR_ETR  | GTMR_CH1     | -         | -   | -         | WAKEUP1            | COMP2_INN                     |
| PB3 | SWCLK (默认) | UART_TX | -       | ATMR_CH3N | GTMR_CH2     | BTMR0_CH0 | -   | -         | -                  | -                             |
| PB4 | SWDIO (默认) | UART_RX | -       | ATMR_CH3  | GTMR_CH3     | BTMR1_CH0 | -   | -         | -                  | -                             |

|      | AF0       | AF1      | AF2      | AF3       | AF4          | AF5       | AF6 | AF7       | Secondary function | Analog                 |
|------|-----------|----------|----------|-----------|--------------|-----------|-----|-----------|--------------------|------------------------|
| PB5  | UART_TX   | SPI_CS   | -        | -         | GTMR_CH2     | -         | -   | COMP2_OUT | -                  | ADC_IN6<br>COMP3_INN   |
| PB6  | UART_RX   | SPI_SCK  | I2C_SMBA | -         | GTMR_CH3     | -         | -   | COMP3_OUT | -                  | ADC_IN7<br>COMP123_INP |
| PB7  | UART_TX   | SPI_MISO | I2C_SCL  | -         | GTMR_CH1     | BTMR0_CH0 | -   | COMP1_OUT | -                  | -                      |
| PB8  | UART_RX   | SPI_MOSI | I2C_SDA  | -         | GTMR_CH0_ETR | BTMR1_CH0 | -   | -         | -                  | -                      |
| PB9  | USART_TX  | SPI_CS   | -        | ATMR_BKIN | GTMR_CH3     | -         | -   | COMP2_OUT | -                  | COMP0_INP              |
| PB10 | USART_RX  | SPI_SCK  | -        | ATMR_ETR  | GTMR_CH0_ETR | -         | -   | COMP0_OUT | -                  | -                      |
| PB11 | USART_CTS | SPI_MISO | -        | ATMR_CH3N | GTMR_CH1     | BTMR0_CH0 | -   | COMP1_OUT | -                  | -                      |
| PB12 | USART_RTS | SPI_MOSI | -        | ATMR_CH3  | GTMR_CH2     | BTMR1_CH0 | -   | COMP2_OUT | -                  | ADC_IN5                |

Table 10 Configuration of the GPIOA\_AF3RMP register

|          |                    |                                                                                                                        |
|----------|--------------------|------------------------------------------------------------------------------------------------------------------------|
| bit10:8  | PA10 PWM multiplex | 000,110,111: ATMR_CH0<br>001: ATMR_CH1<br>010: ATMR_CH2<br>011: ATMR_CH0N<br>100: ATMR_CH1N<br>101: ATMR_CH2N(Default) |
| bit14:12 | PA11 PWM multiplex | 000,110,111: ATMR_CH0<br>001: ATMR_CH1<br>010: ATMR_CH2(Default)<br>011: ATMR_CH0N<br>100: ATMR_CH1N<br>101: ATMR_CH2N |

|          |                    |                                                                                                                        |
|----------|--------------------|------------------------------------------------------------------------------------------------------------------------|
| bit10:8  | PA10 PWM multiplex | 000,110,111: ATMR_CH0<br>001: ATMR_CH1<br>010: ATMR_CH2<br>011: ATMR_CH0N<br>100: ATMR_CH1N<br>101: ATMR_CH2N(Default) |
| bit18:16 | PA12 PWM multiplex | 000,110,111: ATMR_CH0<br>001: ATMR_CH1<br>010: ATMR_CH2<br>011: ATMR_CH0N<br>100: ATMR_CH1N(Default)<br>101: ATMR_CH2N |
| bit22:20 | PA13 PWM multiplex | 000,110,111: ATMR_CH0<br>001: ATMR_CH1(Default)<br>010: ATMR_CH2<br>011: ATMR_CH0N<br>100: ATMR_CH1N<br>101: ATMR_CH2N |
| bit26:24 | PA14 PWM multiplex | 000,110,111: ATMR_CH0<br>001: ATMR_CH1<br>010: ATMR_CH2<br>011: ATMR_CH0N(Default)<br>100: ATMR_CH1N<br>101: ATMR_CH2N |

|          |                    |                                                                                                                           |
|----------|--------------------|---------------------------------------------------------------------------------------------------------------------------|
| bit10:8  | PA10 PWM multiplex | 000,110,111: ATMR_CH0<br>001: ATMR_CH1<br>010: ATMR_CH2<br>011: ATMR_CH0N<br>100: ATMR_CH1N<br>101: ATMR_CH2N(Default)    |
| bit31:28 | PA15 PWM multiplex | 000,110,111:<br>ATMR_CH0(Default)<br>001: ATMR_CH1<br>010: ATMR_CH2<br>011: ATMR_CH0N<br>100: ATMR_CH1N<br>101: ATMR_CH2N |

Note:

- (1) all IO support 5V.
- (2) In F031, PA10 to PA15 multiplex by GPIOA\_AF3RMP register other ATMR channel configuration.
- (3) In M3122/M3114/M3115, PA10 to PA15 are connected to HINx/LINx at will.
- (4) In M3122, PB12 is connected to VDET.
- (5) If PA0 and PA5 are not used as OPAMP output functions, they can serve as direct detection channels for the ADC. For specific configuration details, please refer to the description of ADC channel selection in the user manual.

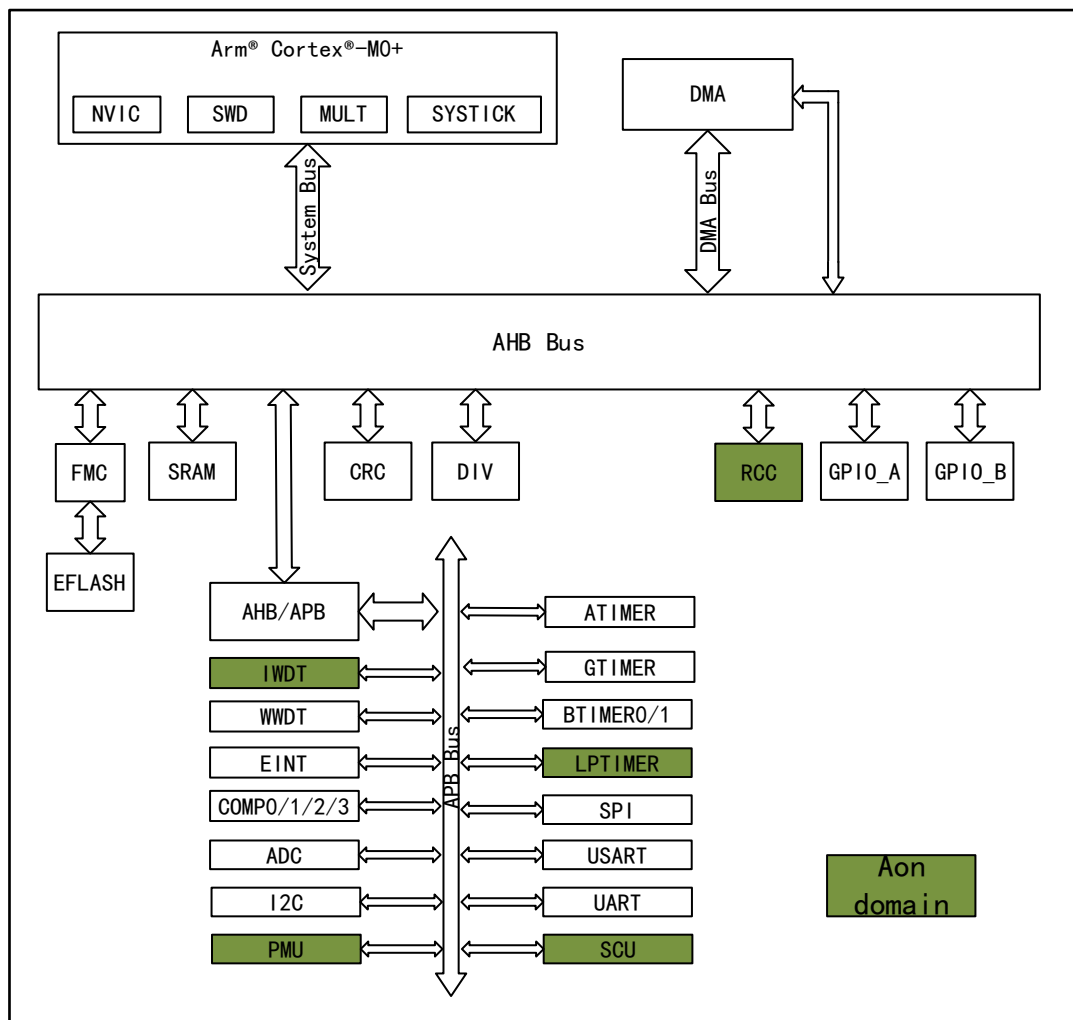
## 6 Functional Description

This chapter mainly introduces the system architecture, interrupt, on-chip memory, clock, power supply and peripheral features of G32F031/M3122/M3114/M3115 series of products. For information about the Arm® Cortex®-M0+ core, refer to the *Arm® Cortex®-M0+ Technical Reference Manual*, which can be downloaded from Arm's website.

### 6.1 System Architecture

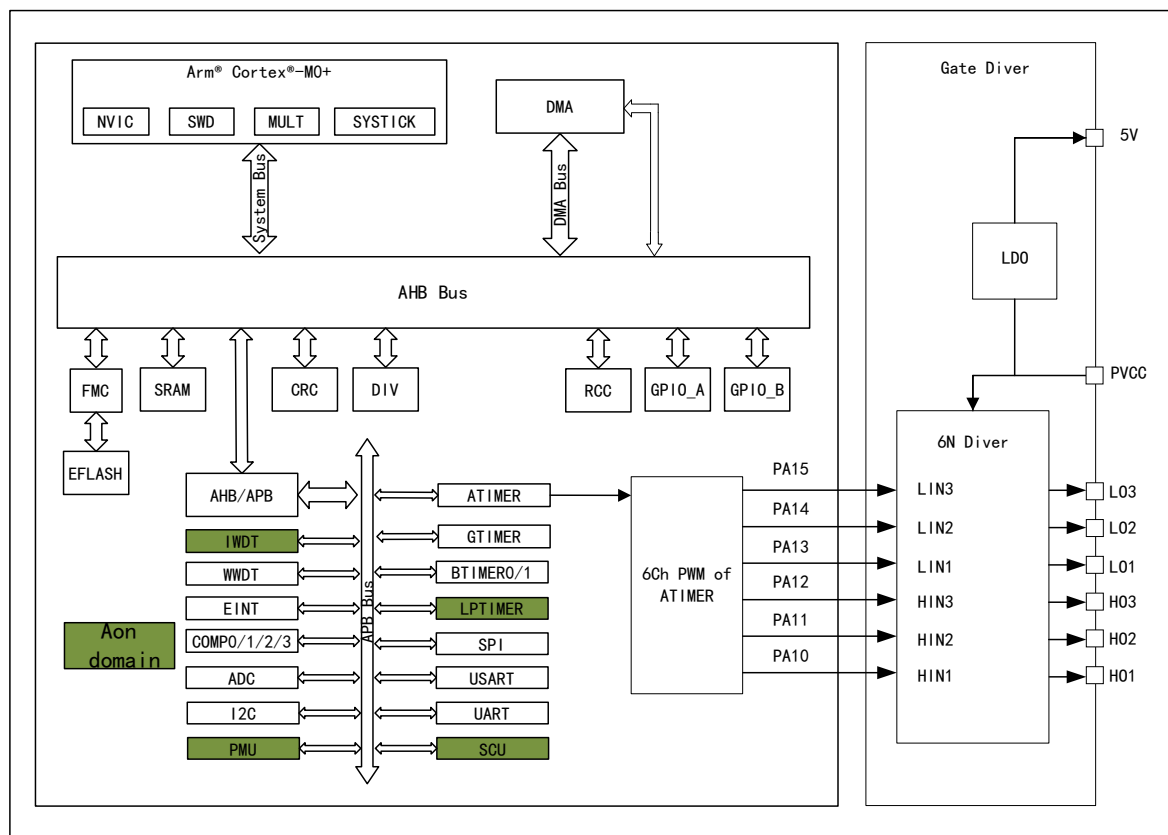
#### 6.1.1 System Block Diagram for F031

Figure 13 System Block Diagram



## 6.1.2 System Block Diagram for M3114

Figure 14 System Block Diagram



## 6.1.3 Logic truth value of the drive

- (1) VBS undervoltage will only set the HO output low.
- (2) VCC undervoltage will set both LO and HO outputs low.
- (3) The VG signal is pulled up to high by default, and the LDO output is turned off when the external pull-down is low.
- (4) After the over temperature protection function is triggered, both the drive output and LDO output are turned off.

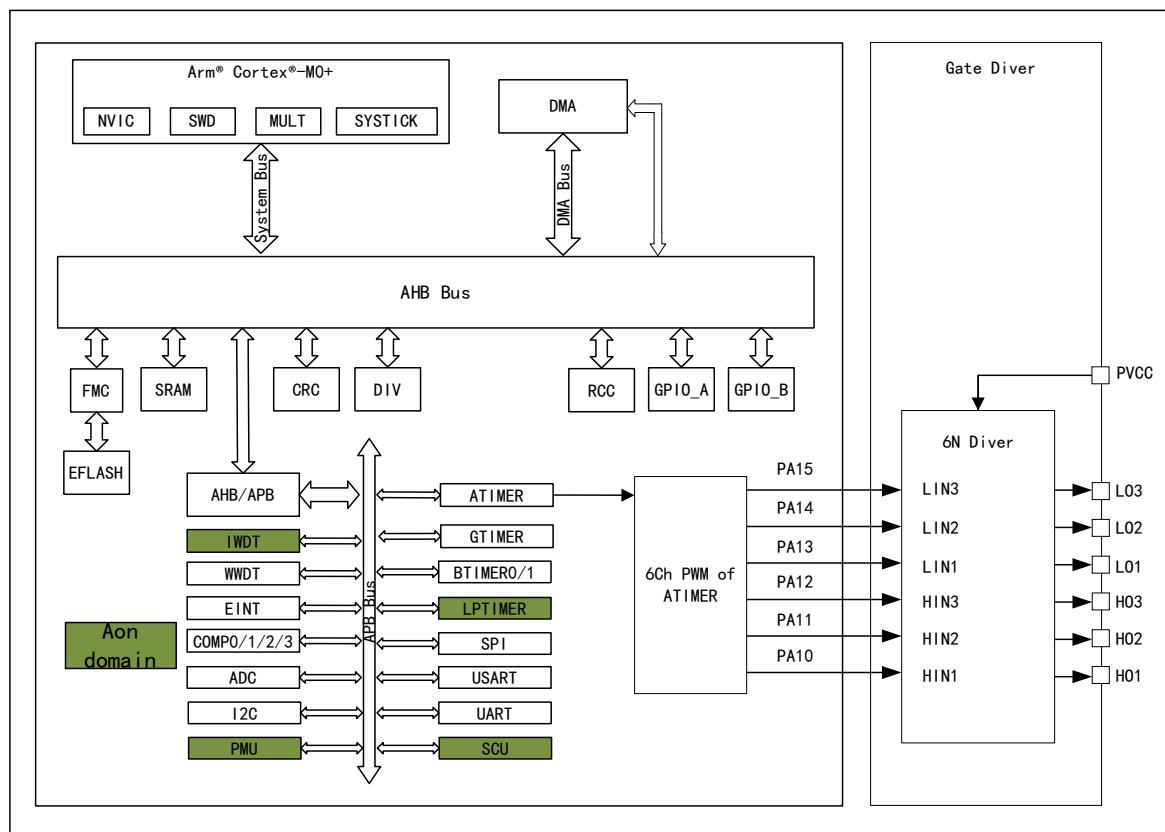
Table 11 Logic truth value of the drive

| OTP    | VG     | VCCUV  | VBSUV  | LIN | HIN | LO  | HO  | LDO |
|--------|--------|--------|--------|-----|-----|-----|-----|-----|
| normal | normal | normal | normal | L   | H   | L   | H   | 5V  |
| normal | normal | normal | normal | H   | L   | H   | L   | 5V  |
| normal | normal | normal | normal | L   | L   | L   | L   | 5V  |
| normal | normal | normal | normal | H   | H   | L   | L   | 5V  |
| normal | normal | normal | UV     | H&L | H&L | H&L | L   | 5V  |
| normal | normal | UV     | normal | H&L | H&L | L   | L   | 5V  |
| normal | L      | normal | normal | H&L | H&L | H&L | H&L | 0V  |

|      |        |        |        |     |     |   |   |    |
|------|--------|--------|--------|-----|-----|---|---|----|
| OVER | normal | normal | normal | H&L | H&L | L | L | 0V |
|------|--------|--------|--------|-----|-----|---|---|----|

### 6.1.1 System Block Diagram for M3115

Figure 15 System Block Diagram



### 6.1.2 Logic truth value of the drive

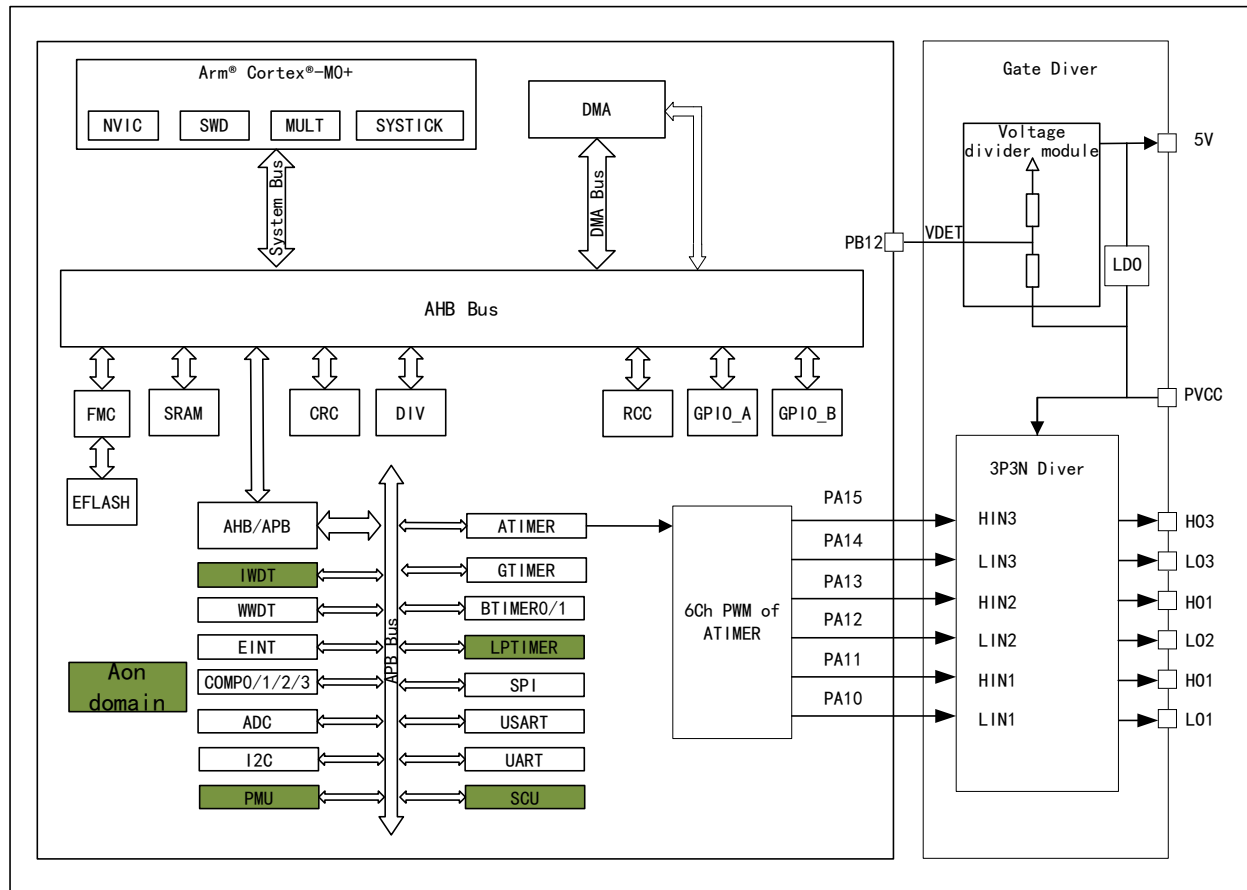
Table 12 Logic truth value of the drive

| VCCUV       | VBSUV       | LIN | HIN | LO | HO |
|-------------|-------------|-----|-----|----|----|
| normal      | normal      | L   | H   | L  | H  |
| normal      | normal      | H   | L   | H  | L  |
| normal      | normal      | L   | L   | L  | L  |
| normal      | normal      | H   | H   | L  | L  |
| under vccuv | normal      | L   | H   | L  | L  |
| under vccuv | normal      | H   | L   | L  | L  |
| under vccuv | normal      | L   | L   | L  | L  |
| under vccuv | normal      | H   | H   | L  | L  |
| normal      | under vbsuv | L   | H   | L  | L  |
| normal      | under vbsuv | H   | L   | H  | L  |
| normal      | under vbsuv | L   | L   | L  | L  |

|        |             |     |     |    |    |
|--------|-------------|-----|-----|----|----|
| VCCUV  | VBSUV       | LIN | HIN | LO | HO |
| normal | under vbsuv | H   | H   | L  | L  |

### 6.1.3 System Block Diagram for M3122

Figure 16 System Block Diagram



### 6.1.4 Logic truth value of the drive

Table 13 Logic truth value of the drive

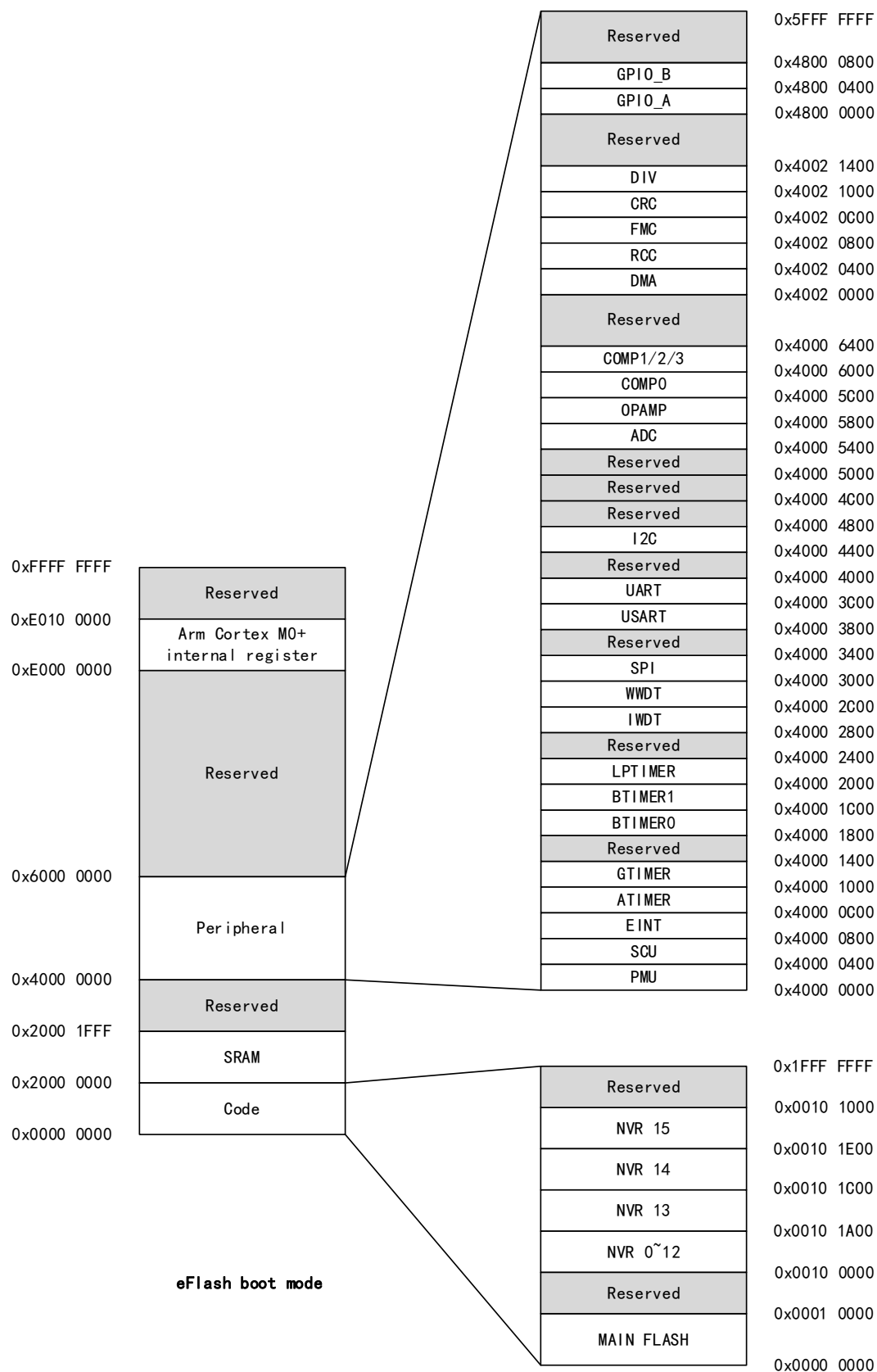
| LIN        | HIN        | LO  | HO  |
|------------|------------|-----|-----|
| 0          | 0          | OFF | OFF |
| 0          | 1          | OFF | ON  |
| 1          | 0          | ON  | OFF |
| 1          | 1          | OFF | OFF |
| Suspension | Suspension | OFF | OFF |

Note:

- (1) 1: Logic high level, 0: Logic low level.
- (2) ON:  $V_{HO}=V_{SUP1}-11V$ ,  $V_{LO}=11V$  OFF:  $V_{HO}=V_{SUP1}$ ,  $V_{LO}=0V$ .
- (3) It is recommended to maintain a strong input state at the input port to avoid unstable states such as high resistance and suspension.

## 6.1.5 Address Mapping

Figure 17 Address Mapping



### 6.1.6 Start boot mode

The chip is activated by the Main memory (Main Flash). The main memory is mapped to the boot space, but it can still be accessed at its original address, that is, the contents of the flash memory can be accessed in two address areas.

## 6.2 Core

The core of G32F031/M3122/M3114/M3115 is Arm® Cortex®-M0+, with its own MULT. based on a platform with low development cost, low power consumption, excellent computing performance and advanced system interrupt response. It is compatible with all Arm tools and software.

## 6.3 Interrupt controller

### 6.3.1 Nested Vector Interrupt Controller (NVIC)

1 built-in NVIC and it is capable of handling up to 32 maskable interrupt channels and 4 priority levels. It can pass the interrupt vector entry address directly to the core to achieve low-latency interrupt response processing to prioritize the late arrival of higher priority interrupts.

### 6.3.2 External Interrupt/Event Controller (EINT)

External interrupt/event controller has 18 edge detectors, each detector contains edge detection circuitry, interrupt/event request generation circuitry; each detector can be configured as a rising-edge triggered, falling-edge, double-edge triggered, but also able to individually mask. Up to 29 GPIOs can be connected to 16 external interrupt lines.

## 6.4 On-chip memory

The on-chip memory includes the main storage area, SRAM, and user area.

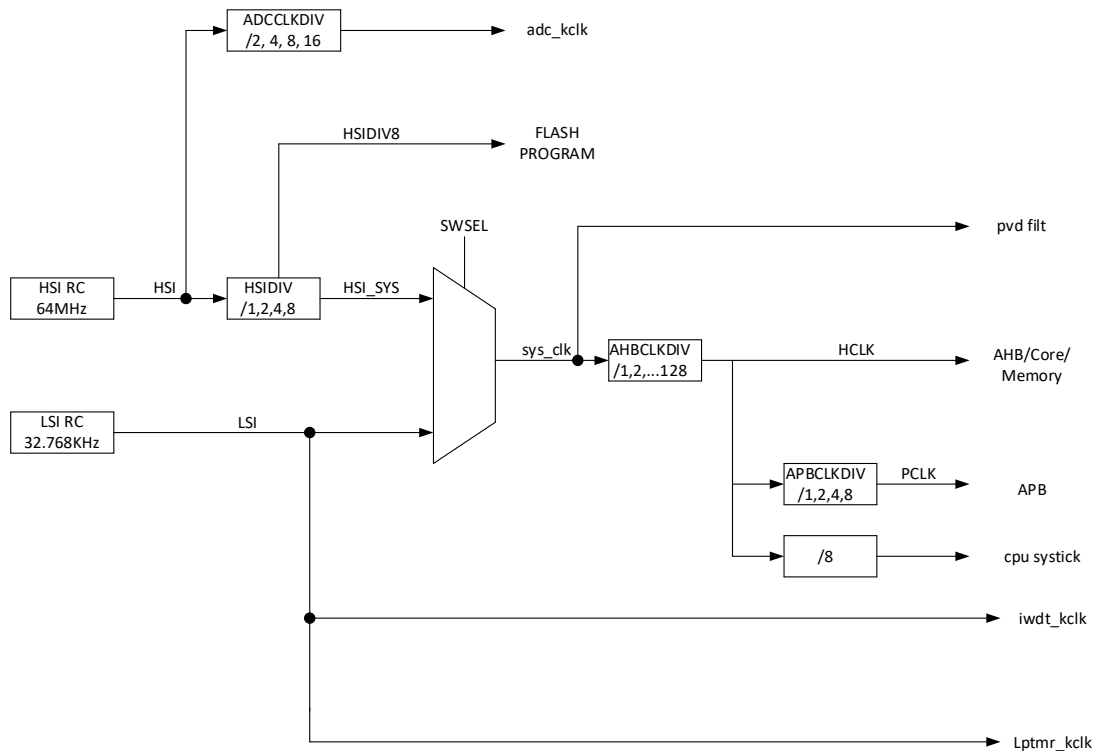
Table 14 On-chip Memory

| Memory           | Maximum Capacity | Function                                                   |
|------------------|------------------|------------------------------------------------------------|
| Main memory area | 64KB             | Storage for user programme and data                        |
| SRAM             | 8 KB             | CPU can access (read/write) with 0 cycles                  |
| User area        | 512 Bytes        | Configuration of read/write protection of main memory area |

## 6.5 Clock

### 6.5.1 Clock tree

Figure 18 Clock Tree



### 6.5.2 Clock sources

Clock source is divided into high-speed clock HSICLK and low-speed clock LSICLK according to the speed. In addition, some modules have additional clock source pins to obtain the required clock frequency through external circuits.

### 6.5.3 System clock

When the product is reset and started, HSICLK is started as the system clock by default, and if the interrupt is enabled, the software can receive the corresponding interrupt.

### 6.5.4 Bus clock

Built-in AHB, APB bus, the clock source of AHB is SYSCLK, and the clock source of APB is HCLK. Configure the dividing coefficient to obtain the required clock. The maximum frequency of AHB and APB is 64 MHz.

## 6.6 Power and power management

### 6.6.1 Power solution

Table 15 Power Supply Scheme

| Name            | Voltage range | Description                                                                                                   |
|-----------------|---------------|---------------------------------------------------------------------------------------------------------------|
| V <sub>DD</sub> | 1.8~5.5V      | Supplies power to I/O (see pin diagram for specific I/O), and internal regulator through V <sub>DD</sub> pin. |

Note: It is recommended to use 10uF and 100nF capacitors in parallel at the V<sub>DD</sub> terminal.

### 6.6.2 Voltage regulator

Table 16 Regulator Operating Mode

| Name                 | Description       |
|----------------------|-------------------|
| Master mode (MR)     | Used in run mode  |
| Low-power mode (LPR) | Used in stop mode |

Note: The regulator is always in working state after reset.

### 6.6.3 Power supply voltage detector

Power-on reset (POR), power-down reset (PDR) are integrated inside the product. These two circuits are always in working condition. When the power-down reset circuit detects that the power supply voltage is lower than the specified threshold value (V<sub>POR/PDR</sub>), even if the external reset circuit is used, the system will remain reset.

The product has a built-in programmable voltage detector (PVD) that monitors V<sub>DD</sub> and compares it to the V<sub>PVD</sub> threshold, and generates an interrupt when V<sub>DD</sub> is outside of the V<sub>PVD</sub> threshold range. The MCU can be set to a safe state through the interrupt service.

## 6.7 Low power mode

G32F031/M3122/M3114/M3115 supports three low-power modes, which are sleep mode, stop mode and standby mode. There are differences in power consumption, wake-up time and wake-up mode among these three modes. The low-power mode can be selected according to the actual requirements.

Table 17 Low Power Mode

| Mode         | Description                                                                                                                                                                                                                                                                                                                                                  |
|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Sleep mode   | The core stops working, all peripherals are working, and it can be woken up through interrupts/events                                                                                                                                                                                                                                                        |
| Stop mode    | Under the condition that SRAM and register data are not lost, the lowest power consumption can be achieved in stop mode.<br>The clock of the internal 5V power supply stops. HSICLK is disabled, and LSICLK is enabled. The voltage regulator can be configured to normal mode or low-power mode.<br>The MCU can be woken up by any external interrupt line. |
| Standby mode | The power in this mode is the lowest;                                                                                                                                                                                                                                                                                                                        |

| Mode | Description                                                                                                                                                                                                                                                                                                                          |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      | <p>The internal voltage regulator is disabled, all 1.5V power supply modules are powered down, LSICLK and HSICLK clocks are disabled, SRAM and register data disappears, and the standby circuit still works;</p> <p>The external reset signal on NRST, edge on WKUP pin or RTC event will wake up MCU to exit the standby mode.</p> |

## 6.8 DMA

A built-in DMA supports two DMA channels, each channel supports multiple DMA requests, but only one DMA request is allowed to enter the DMA channel at the same time. The peripherals supporting DMA requests are ADC, SPI, I2C, USART, UART, GTMR. Five levels of DMA channel priority can be configured, and data transmission of "Memory → Memory, Memory → Peripheral, Peripheral → Memory" can be supported (memory includes Flash and SRAM).

## 6.9 GPIO

The maximum driving capability of GPIO is 6mA. It can be configured as general input mode, general output mode, multiplexing function mode, and analog input and output mode. General-purpose input can be configured as high-impedance. General-purpose output can be configured as push-pull and open-drain output. Multiplexing functions can be used for digital peripherals. Analog input and output can be used for analog peripherals as well as for low-power modes. Pull-up/down resistors can be configured to enable/disable the pull-up/pull-down resistors. A maximum of 20MHz can be configured, and the higher the speed, the larger the power consumption and the higher the noise will be. Supports schmitt inputs.

## 6.10 Communication peripherals

### 6.10.1 USART/UART

1 built-in general-purpose synchronous/asynchronous transceiver and 1 general-purpose asynchronous transceiver, with the communication rate at 8Mbit/s. All USART/UART can be configured with baud rate, parity bit, stop bit, data bit length, and can support DMA. The comparison of various USART/UART functions is shown in the table below:

Table 18 Comparison of supported functions between USART and UART

| USART Mode                                              | USART | UART |
|---------------------------------------------------------|-------|------|
| Half-duplex (single-line mode)                          | √     | √    |
| Automatic baud rate detection                           | √     | √    |
| Multiprocessor communication                            | √     | -    |
| Wake up from mute mode                                  | √     | -    |
| The maximum baud rate at 16 times oversampling (Mbit/s) | 4     | 4    |
| The maximum baud rate at 8 times oversampling (Mbit/s)  | 8     | -    |

| USART Mode                       | USART | UART |
|----------------------------------|-------|------|
| Synchronization mode             | √     | -    |
| LIN mode                         | √     | √    |
| Hardware flow control            | √     | -    |
| RS485 driver enable              | √     | -    |
| Multi-buffer communication (DMA) | √     | √    |
| Receiver timeout interrupt       | √     | √    |
| Modbus communication             | √     | -    |

Note:√ means support.

## 6.10.2 I2C

I2C bus interfaces are built-in and they all can work in multiple-master or slave modes, supports standard mode (up to 100kbit/s), fast mode (up to 400kbit/s) and fast mode plus (1Mbit/s); and can use DMA controllers. The I2C interface supports 7-bit or 10-bit addressing and dual-address addressing.

In addition, I2C also provides hardware support for SMBUS2.0 and PMBUS1.1: ARP function, master notification protocol, hardware CRC(PEC) generation/verification, timeout verification and alert protocol management.

## 6.10.3 SPI

1 built-in SPI, supports full-duplex and half-duplex communication in both master and slave modes. DMA controller can be used, with a maximum communication rate of 16Mbps.

## 6.11 Analog peripherals

### 6.11.1 ADC

1 built-in ADC with 12-bit accuracy, with up to 8+2 external channels and 5 internal channels. The internal channels measure the temperature sensor voltage and internal reference voltage, OPAMP0/1 and 1/2VDD respectively. The A/D conversion modes of each channel are single, continuous or intermittent, and the ADC conversion results can be left-aligned or right-aligned stored in the data register. Segmented sampling is supported. DMA is supported.

#### 6.11.1.1 Temperature sensor

1 built-in temperature sensor (TSensor), accuracy  $\pm 5^{\circ}\text{C}$ . The voltage generated by the sensor varies linearly with the temperature, and can be converted to temperature by acquiring the converted voltage value from ADC.

Table 19 Tsensor Calibration Value

| Calibration value name  | Description                                                           | Address     |
|-------------------------|-----------------------------------------------------------------------|-------------|
| V <sub>sensor_CAL</sub> | Raw data collected at 25°C, V <sub>DDA</sub> =5V( $\pm 10\text{mV}$ ) | 0x0010 1C14 |

### 6.11.1.2 Internal reference voltage

1 built-in internal reference voltage  $V_{BG}$ , and the  $V_{BG}$  voltage value can be obtained through the ADC. Meanwhile, the internal reference voltage is programmable and can be used as the positive input of COMP and the built-in bias voltage of OPAMP. (Note: There is a conversion relationship between the measured value of  $V_{BG}$  at the storage address and the value  $V_{BG}$  obtained by the ADC through the internal channel. The measured value of  $V_{BG} = 1.2498 * V_{BG}$ )

Table 20 Calibration Value of Internal Reference Voltage

| Calibration value name     | Description                                               | Address     |
|----------------------------|-----------------------------------------------------------|-------------|
| Measured value of $V_{BG}$ | Raw data collected at 25°C (±5°C),<br>$V_{DDA}=5V(±10mV)$ | 0x0010 1C1C |

### 6.11.2 Comparator (COMP)

4 built-in fast rail-to-rail comparators, support internal/external reference voltage, hysteresis, rate, programmable function, and configurable output polarity. Reference voltage can be selected from external I/O, internal reference voltage ( $V_{BG}$ ), internal reference voltage 1/2. It can generate interrupts and simultaneously wake up the Sleep mode.

### 6.11.3 Operational amplifier (OPAMP)

It is equipped with 2 rail-to-rail OPAMPs with magnification ratios of 1,4,6,8,10,12 and 16 times. The output mode can be selected, with built-in biases of 1/2  $V_{DDA}$ , 1/4  $V_{DDA}$ , BG or 1/4 BG.

## 6.12 Timer

1 built-in 16-bit advanced timer ATIMER, 1 32-bit general-purpose timer GTIMER, 2 16-bit basic timer BTIMER, 1 low-power timer LPTIMER, 1 independent watchdog timer, 1 window watchdog timer, and 1 24-bit self-reducing system tick timer.

The watchdog timers can be used to check if a programme is running correctly.

The system tick timer is a peripheral of the core with an auto-reload function that generates a maskable system interrupt when the counter is 0. It can be used for a real-time operating system and time delay.

Table 21 Advanced/General/Basic/Low Power Timer Function Comparison

| Item                | Specific content/<br>Category | Advanced Timer                 | General Timer                  | Basic Timer                    | Low Power<br>Consumption<br>Timer |
|---------------------|-------------------------------|--------------------------------|--------------------------------|--------------------------------|-----------------------------------|
| Name                | -                             | ATIMER                         | GTIMER                         | BTIMER                         | LPTIMER                           |
| Time-<br>based unit | Counter                       | 16-bit                         | 32-bit                         | 16-bit                         | 16-bit                            |
|                     | Prescaler                     | 16-bit                         | 16-bit                         | 16-bit                         | 16-bit                            |
|                     | Counting Mode                 | Up<br>Down<br>Center alignment | Up<br>Down<br>Center alignment | Up<br>Down<br>Center alignment | Up                                |
| Channel             | Input Channel                 | 0                              | 4                              | 1                              | 0                                 |

| Item     | Specific content/<br>Category | Advanced Timer | General Timer | Basic Timer | Low Power<br>Consumption<br>Timer |
|----------|-------------------------------|----------------|---------------|-------------|-----------------------------------|
|          | Capture Compare Channel       | 4              | 4             | 1           | 0                                 |
|          | Output channel                | 8              | 4             | 1           | 0                                 |
|          | Complementary output channel  | 4 groups       | 0             | 0           | 0                                 |
| Function | Generate DMA request          | No             | Yes           | No          | No                                |
|          | PWM mode                      | Yes            | Yes           | Yes         | No                                |
|          | Single pulse mode             | Yes            | Yes           | Yes         | No                                |
|          | Forced output mode            | Yes            | Yes           | Yes         | No                                |
|          | Deadband insertion            | Yes            | No            | No          | No                                |

Table 22 IWDt and WWDt Comparison

| Name | Counter resolution | Counter type | Prescaler factor     | Function description                                                                                                                                                                                                                                                                               |
|------|--------------------|--------------|----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IWDt | 12-bit             | Down         | 4/8/16/32/64/128/256 | The clock provided by an internal independent 32.768KHz RC oscillator. Because this RC oscillator is independent of the main clock, it can operate in stop modes.<br>In case of problems, can reset the system.<br>Can be used as a flexible timer to provide timeout management for applications. |
| WWDt | 7-bit              | Down         | 1/2/4/8              | Can be set to run flexibly.<br>In case of problems, can reset the system.<br>Driven by the main clock with early warning interrupt function.                                                                                                                                                       |

## 6.13 CRC

1 built-in CRC (Cyclic Redundancy Check) computing unit, which can generate CRC codes and can operate on 16-bit, and 32-bit data.

## 6.14 DIV

Include four 32-bit data registers that store divisor, dividend, quotient, and remainder respectively. It supports both signed and unsigned division.

## 6.15 Gate driver

### 6.15.1 M3114

The G32M3114 is embedded with a three-phase medium-voltage high-speed gate driver IC,

which is specially designed for driving double-N-channel VDMOS power transistor or IGBT in bridge circuits, and is suitable for application schemes for battery-powered DC brushless motors. The embedded typical dead time is 500ns. When the dead time of the MCU output signal is less than the embedded dead time, the actual dead time is the embedded dead time. On the contrary, when the dead time of the MCU output signal is greater than the embedded dead time, the actual dead time is the output dead time of MCU. The embedded VCC and VBS undervoltage protection functions can prevent the system from turning on the external power transistors at low driving voltage. The output of the high-side driving circuit and the output of the low-side driving circuit are controlled through input signals. The built-in LDO of the driver supports power supply for control chips such as the MCU, and this LDO supports a 5V voltage output.

#### **6.15.2 Main characteristics**

- Operating supply voltage range: 5~20V
- Floating offset voltage: +200V
- Embedded VCC and VBS undervoltage protection
- Embedded straight-through prevention function
- Embedded input pull-down resistor
- Embedded output pull-down resistor
- Matching the transmission time of high and low-end channels
- High dv/dt noise suppression capability
- Input and output in-phase
- Compatible with 3.3V/5V logic input
- Peak input current 1.1A@15V, 3.3nF load fall time 40ns
- Peak output current 0.9A@15V, 3.3nF load rise time 65ns
- LDO load capacity 60mA@15V
- Overtemperature protection threshold 151℃ /131℃

#### **6.15.3 M3115**

The G32M3115 is embedded with a three-phase medium-voltage high-speed gate driver IC, which is specially designed for driving double-N-channel VDMOS power transistor or IGBT in bridge circuits, and is suitable for application schemes for battery-powered DC brushless motors. The embedded typical dead time is 220ns. When the dead time of the MCU output signal is less than the embedded dead time, the actual dead time is the embedded dead time. On the contrary, when the dead time of the MCU output signal is greater than the embedded dead time, the actual dead time is the output dead time of MCU. The embedded VCC and VBS undervoltage protection functions can prevent the system from turning on the external power transistors at low driving voltage. The output of the high-side driving circuit and the output of the low-side driving circuit are controlled through input signals.

#### **6.15.4 Main characteristics**

- Operating supply voltage range: 5.5~20V
- Floating offset voltage: +200V
- Embedded minimum dead time: 220ns
- Embedded VCC and VBS undervoltage protection

- Embedded straight-through prevention function
- Embedded input pull-down resistor
- Embedded output pull-down resistor
- Matching the transmission time of high and low-end channels
- High dv/dt noise suppression capability
- Input and output in-phase
- Compatible with 3.3V/5V logic input
- Peak output current 2.0A @15V, 3.3 nF load fall time 20 ns
- Peak output current 2.7A@15V, 3.3 nF load rise time 35 ns

#### **6.15.5 M3122**

The G32M3122 integrates a three-phase 40V gate driver integrated circuit for driving P/NMOS power transistors. and is suitable for DC brushless motor applications such as low-voltage fans and water pumps. This chip integrates 5V LDO, has a current-carrying capacity of 60mA, and can provide power for internal logic circuits and external MCU. Multiple protection functions are built in G32M3122, including undervoltage protection, input straight-through protection, and startup protection. It has a dead time of 300ns to effectively ensure normal operation of the system. At the same time, it provides an output driving voltage of 11V, has excellent sink current capability, and can effectively drive the external P/NMOS power transistors.

#### **6.15.6 Main characteristics**

- Three-phase gate driver for P/NMOS power transistors
- Recommended range of supply voltage: 5.5V~30V
- Built-in 5V/60mA LDO
- HO output current+260mA/-80mA@ $V_{sup}=24V$
- LO output current+50mA/-240mA@ $V_{sup}=24V$
- Low standby power consumption
- 3.3V/5V input logic compatibility
- LDO overload start protection
- Built-in power undervoltage protection UVLO
- Built-in straight-through prevention function
- Built-in 300ns dead time
- Matching of high and low-side channels

## **7 Electrical Characteristics**

### **7.1 Test Conditions of Electrical Characteristics**

All voltage parameters (unless otherwise specified) refer to  $V_{SS}$ .

#### **7.1.1 Maximum and Minimum Values**

Unless otherwise specified, all products are tested on the production line at  $T_A=25^{\circ}\text{C}$ . Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

In the notes at the bottom of each table, it is stated that the data obtained through comprehensive evaluation, design simulation or process characteristics are not tested on the production line. On the basis of comprehensive evaluation, take the average value and add and subtract three times the standard deviation (average  $\pm 3\Sigma$ ) to get the maximum and minimum values after passing the sample test.

#### **7.1.2 Typical values**

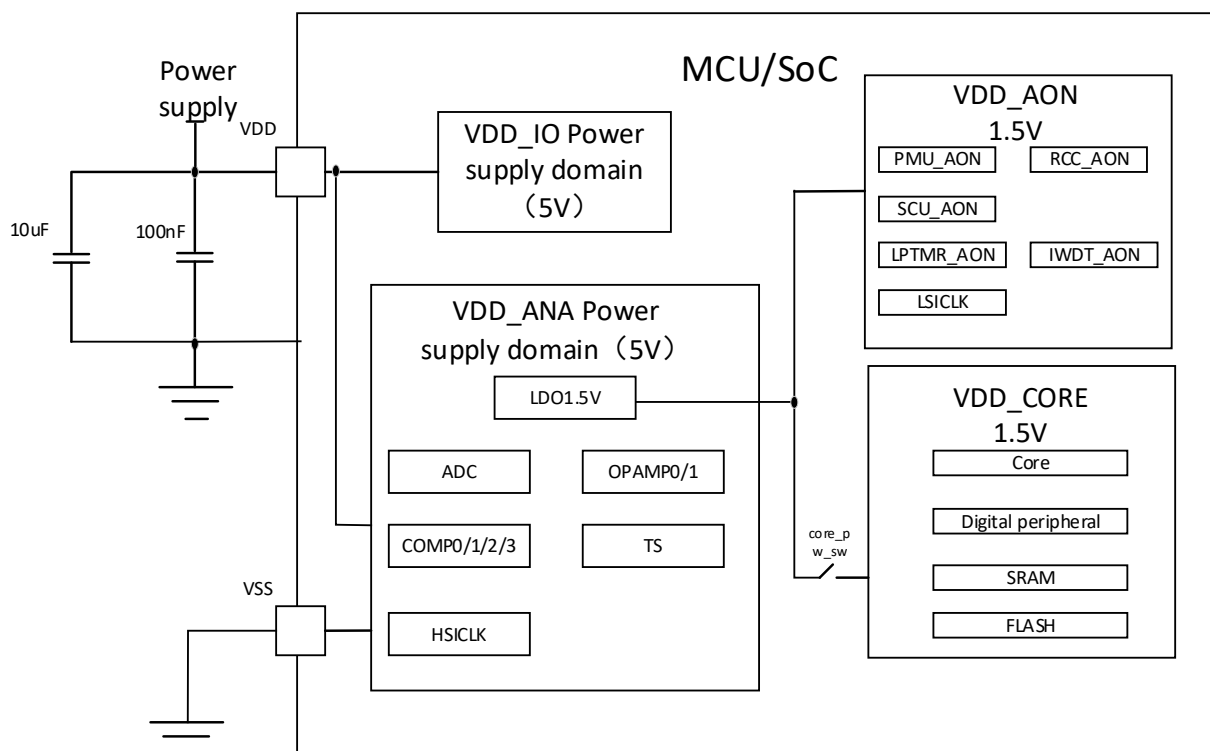
Unless otherwise specified, typical data are measured based on  $T_A=25^{\circ}\text{C}$ ,  $V_{DD}=5\text{V}$ . these data are only used for design guidance.

#### **7.1.3 Typical curve**

Unless otherwise specified, typical curves will not be tested on the production line, and will only be used for design guidance.

## 7.1.4 Power Supply Scheme

Figure 19 Power Supply Scheme



## 7.1.5 Load Capacitance

Figure 20 Load Conditions when Measuring Pin Parameters

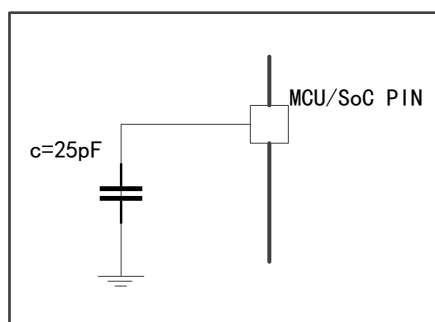


Figure 21 Pin Input Voltage Measurement Scheme

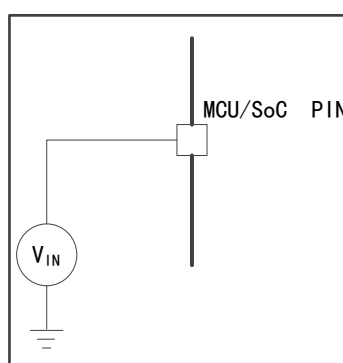
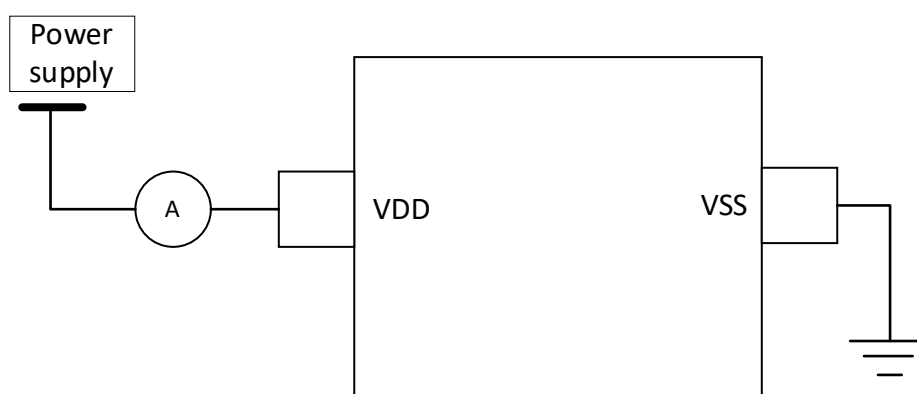


Figure 22 Power Consumption Measurement Scheme



## 7.2 Testing under General Working Conditions

Table 23 General Working Conditions

| Symbol            | Parameter                    | Condition | Min  | Max                  | Unit |
|-------------------|------------------------------|-----------|------|----------------------|------|
| f <sub>HCLK</sub> | Internal AHB clock frequency | -         | -    | 64                   | MHz  |
| f <sub>PCLK</sub> | Internal APB clock frequency | -         | -    | 64                   |      |
| V <sub>DD</sub>   | Power supply voltage input   | -         | 1.8  | 5.5                  | V    |
| V <sub>IN</sub>   | I/O input voltage            | -         | -0.3 | V <sub>DD</sub> +0.3 | V    |

## 7.3 Absolute Maximum Rating

If the load on the device exceeds the absolute maximum rating, it may cause permanent damage to the device. Here, only the maximum load that can be borne is given, and there is no guarantee that the device functions normally under this condition.

### 7.3.1 Maximum Temperature Characteristics

Table 24 Temperature Characteristics

| Symbol           | Description                  | Numerical value | Unit |
|------------------|------------------------------|-----------------|------|
| T <sub>STG</sub> | Storage temperature range    | -65~150         | °C   |
| T <sub>J</sub>   | Maximum junction temperature | 125             | °C   |

### 7.3.2 Maximum Rated Voltage Characteristics

All power supply and ground pins must always be connected to the power supply within the external limited range.

Table 25 Maximum Rated Voltage Characteristics

| Symbol          | Description                | Min  | Max | Unit |
|-----------------|----------------------------|------|-----|------|
| V <sub>DD</sub> | Power supply voltage input | -0.3 | 6   | V    |

### 7.3.3 Maximum Rated Current Characteristics

Table 26 Maximum Rated Current Characteristics

| Symbol                | Description                                                          | Max  | Unit |
|-----------------------|----------------------------------------------------------------------|------|------|
| $\Sigma I_{VDD}$      | Total current into sum of all $V_{DD}$ power lines <sup>(1)</sup>    | 75   | mA   |
| $\Sigma I_{VSS}$      | Total current out of sum of all $V_{SS}$ ground lines <sup>(1)</sup> | 75   |      |
| $I_{IO(PIN)}$         | Output current sunk by any I/O and control pin                       | +6   |      |
|                       | Output current source by any I/O and control pin                     | -6   |      |
| $I_{INJ(PIN)}^{(2)}$  | Injected current on NRST pins                                        | 0/+6 |      |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (other pins) <sup>(3)</sup>                   | ±24  |      |

- (1) All main power and ground pins must always be within the permitted range.
- (2) If  $V_{IN}$  exceeds its maximum value, an external limit must be imposed on  $I_{INJ(PIN)}$  not to exceed its maximum value. When  $V_{IN} > V_{DDIOX}$ , current flows into the pin. When  $V_{IN} < V_{SS}$ , current flows out of the pin.
- (3) When several inputs are submitted to a current injection, the maximum  $\Sigma I_{INJ(PIN)}$  is the absolute sum of the positive and negative injected currents (instantaneous values).

### 7.3.4 ESD Characteristics

Table 27 ESD Characteristics

| Symbol         | Parameter                                                  | Condition                                                            | Max  | Unit |
|----------------|------------------------------------------------------------|----------------------------------------------------------------------|------|------|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (manikin)                  | $T_A = +25^\circ\text{C}$ , Standard:<br>ANSI/ESDA/JEDEC JS-001-2017 | 4000 | V    |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charging equipment model) | $T_A = +25^\circ\text{C}$ , Standard:<br>ANSI/ESDA/JEDEC JS-002-2018 | 2000 |      |

Note: It is tested by a third-party testing organization instead of in production.

### 7.3.5 Latch-up

Table 28 Latch-up

| Symbol | Parameter             | Condition                 | Max        |
|--------|-----------------------|---------------------------|------------|
| LU     | Class of static latch | $T_A = 105^\circ\text{C}$ | Class II A |

Note: It is tested by a third-party testing organization instead of in production.

## 7.4 On-Chip Memory

### 7.4.1 Flash Characteristics

Table 29 Flash Characteristics

| Symbol     | Parameter               | Condition                          | Min | Typ | Max | Unit          |
|------------|-------------------------|------------------------------------|-----|-----|-----|---------------|
| $t_{prog}$ | 32 bit programming time | $T_A = -40 \sim 105^\circ\text{C}$ | -   | 60  | -   | $\mu\text{s}$ |

| Symbol             | Parameter             | Condition                | Min  | Typ  | Max | Unit   |
|--------------------|-----------------------|--------------------------|------|------|-----|--------|
| t <sub>ERASE</sub> | Page(512B) erase time | T <sub>A</sub> =-40~105℃ | -    | 2.45 | -   | ms     |
| t <sub>ME</sub>    | Whole erase time      | T <sub>A</sub> =25℃      | -    | 30   | -   | ms     |
| V <sub>prog</sub>  | Programming voltage   | T <sub>A</sub> =-40~105℃ | 2    | -    | 5.5 | V      |
| t <sub>RET</sub>   | Data saving time      | T <sub>A</sub> = 125℃    | 10   | -    | -   | years  |
| N <sub>RW</sub>    | Erase cycle           | T <sub>A</sub> =-40~105℃ | 100K | -    | -   | cycles |

Note: It is tested in comprehensive evaluation instead of in production.

## 7.5 Clock System

### 7.5.1 Characteristics of Internal Clock Source

#### High speed internal (HSICLK)RC oscillator

Table 30 HSICLK Oscillator Characteristics

| Symbol                  | Parameter                                 | Condition                                       |                                                            | Min  | Typ | Max | Unit |
|-------------------------|-------------------------------------------|-------------------------------------------------|------------------------------------------------------------|------|-----|-----|------|
| f <sub>HSICLK</sub>     | Frequency                                 | -                                               |                                                            | -    | 64  | -   | MHz  |
| A <sub>CCHSICLK</sub>   | Accuracy of HSICLK<br>oscillat            | Factory<br>calibration                          | V <sub>DD</sub> =5V,<br>T <sub>A</sub> =25℃ <sup>(1)</sup> | -0.5 | -   | 0.5 | %    |
|                         |                                           |                                                 | V <sub>DD</sub> =2-5.5V,<br>T <sub>A</sub> =-40~105℃       | -3   | -   | 3   | %    |
|                         |                                           |                                                 | V <sub>DD</sub> =1.8-2V,<br>T <sub>A</sub> =-40~105℃       | -5   | -   | 5   | %    |
| t <sub>SU(HSICLK)</sub> | Startup time of<br>HSICLK oscillator      | V <sub>DD</sub> =5V<br>T <sub>A</sub> =-40~105℃ |                                                            | -    | -   | 10  | μs   |
| I <sub>DD(HSICLK)</sub> | Power consumption of<br>HSICLK oscillator | -                                               |                                                            | -    | 350 | 499 | μA   |

Note: Except for (1) calibration in production, other data are obtained in comprehensive evaluation instead of in production.

#### Low speed internal (LSICLK)RC oscillator

Table 31 LSICLK Oscillator Characteristics

| Symbol                  | Parameter                              | Condition                                           | Min | Typ    | Max  | Unit |
|-------------------------|----------------------------------------|-----------------------------------------------------|-----|--------|------|------|
| f <sub>LSICLK</sub>     | Frequency                              | V <sub>DD</sub> =5V, T <sub>A</sub> =25℃            | 31  | 32.768 | 34   | KHz  |
| t <sub>SU(LSICLK)</sub> | Startup time of LSICLK oscillator      | V <sub>DD</sub> =1.8~5.5V, T <sub>A</sub> =-40~105℃ | -   | 75     | -    | μs   |
| A <sub>CC(LSICLK)</sub> | Accuracy of LSICLK oscillator          |                                                     | -30 | -      | 30   | %    |
| I <sub>DD(LSICLK)</sub> | Power consumption of LSICLK oscillator |                                                     | -   | 0.62   | 0.65 | μA   |

Note: It is tested in comprehensive evaluation instead of in production.

## 7.6 Power Management

### 7.6.1 Power-on/power-down characteristics

Table 32 Power-on/power-down Characteristics

| Symbol    | Parameter               | Condition | Min | Typ | Max    | Unit            |
|-----------|-------------------------|-----------|-----|-----|--------|-----------------|
| $t_{VDD}$ | $V_{DD}$ rise time rate | -         | 10  | -   | 200000 | $\mu\text{s/V}$ |
|           | $V_{DD}$ fall time rate |           | 20  | -   | 200000 |                 |

### 7.6.2 Characteristic test of embedded reset and power control module

Table 33 Embedded Reset and Power Control Module Characteristics

| Symbol              | Parameter                           | Condition    | Min   | Typ   | Max   | Unit |
|---------------------|-------------------------------------|--------------|-------|-------|-------|------|
| $V_{POR/PDR}^{(1)}$ | Power-on/power-down reset threshold | Falling edge | 1.542 | 1.625 | 1.686 | V    |
|                     |                                     | Rising edge  | 1.594 | 1.676 | 1.738 | V    |
| $V_{PDRhyst}$       | PDR hysteresis                      | -            | -     | 50    | -     | mV   |
| LVD                 | -                                   | -            | 1.67  | -     | 1.80  | V    |

Note: It is tested in comprehensive evaluation instead of in production.

(1) PDR detector monitors  $V_{DD}$  and  $V_{DDA}$  (if enabled in option byte), POR detector monitors  $V_{DD}$  only.

Table 34 Programmable Voltage Detector Characteristics

| Symbol    | Parameter                                        | Condition                   | Min  | Typ  | Max  | Unit |
|-----------|--------------------------------------------------|-----------------------------|------|------|------|------|
| $V_{PVD}$ | Level selection of programmable voltage detector | PLS[2:0]=000 (rising edge)  | 1.96 | 2.00 | 2.05 | V    |
|           |                                                  | PLS[2:0]=000 (falling edge) | 1.86 | 1.90 | 1.95 | V    |
|           |                                                  | PLS[2:0]=001 (rising edge)  | 2.35 | 2.40 | 2.46 | V    |
|           |                                                  | PLS[2:0]=001 (falling edge) | 2.25 | 2.30 | 2.36 | V    |
|           |                                                  | PLS[2:0]=010 (rising edge)  | 2.74 | 2.80 | 2.87 | V    |
|           |                                                  | PLS[2:0]=010 (falling edge) | 2.64 | 2.70 | 2.77 | V    |
|           |                                                  | PLS[2:0]=011 (rising edge)  | 3.13 | 3.20 | 3.28 | V    |
|           |                                                  | PLS[2:0]=011 (falling edge) | 3.03 | 3.10 | 3.18 | V    |
|           |                                                  | PLS[2:0]=100 (rising edge)  | 3.52 | 3.60 | 3.69 | V    |
|           |                                                  | PLS[2:0]=100 (falling edge) | 3.42 | 3.50 | 3.58 | V    |
|           |                                                  | PLS[2:0]=101 (rising edge)  | 3.91 | 4.01 | 4.11 | V    |
|           |                                                  | PLS[2:0]=101 (falling edge) | 3.81 | 3.90 | 4.00 | V    |
|           |                                                  | PLS[2:0]=110 (rising edge)  | 4.30 | 4.40 | 4.51 | V    |

| Symbol               | Parameter      | Condition                   | Min  | Typ  | Max  | Unit |
|----------------------|----------------|-----------------------------|------|------|------|------|
|                      |                | PLS[2:0]=110 (falling edge) | 4.20 | 4.30 | 4.41 | V    |
|                      |                | PLS[2:0]=111 (rising edge)  | 4.68 | 4.80 | 4.91 | V    |
|                      |                | PLS[2:0]=111 (falling edge) | 4.59 | 4.70 | 4.81 | V    |
| V <sub>PVDhyst</sub> | PVD hysteresis | -                           | -    | 100  | -    | mV   |

Note: It is tested in comprehensive evaluation instead of in production.

### 7.6.3 BG

Table 35 BG characteristics

| Symbol            | Parameter                                                            | Condition                                       | Min  | Typ | Max  | Unit  |
|-------------------|----------------------------------------------------------------------|-------------------------------------------------|------|-----|------|-------|
| VBG               | BG voltage                                                           | V <sub>DD</sub> =5.5V, T <sub>A</sub> =-40~105℃ | 1.19 | -   | 1.27 | V     |
| I <sub>bias</sub> | BG current                                                           |                                                 | -    | 2   | -    | μA    |
| TS_BG             | Sampling time of the ADC when reading the internal reference voltage | -                                               | 10   | -   | -    | μs    |
| VBG_s             | Built-in reference voltage extends to the temperature range          | V <sub>DD</sub> =5V                             | -    | 5   | 10   | mV    |
| Tcoeff            | Temperature coefficient                                              | -                                               | -    | 50  | 100  | ppm/℃ |

## 7.7 Power Consumption

### 7.7.1 Power consumption test environment

- (1) Test under the conditions of Coremark, KeilV5 compiling environment and L3 compiling optimization level.
- (2) All I/O pins are configured as analog inputs, which are connected to VDD or V<sub>SS</sub> (non-load) at a static level.
- (3) Unless otherwise specified, all peripherals are turned off.
- (4) The relationship between the setting of flash waiting period and f<sub>HCLK</sub>:  
 0~16MHz: 0 waiting periods,  
 16~32MHz: 1 waiting periods,  
 32~64MHz: 2 waiting periods.
- (5) Instruction prefetch function is enabled (Note: this bit must be set before clock setting and bus frequency division).
- (6) When the peripheral is turned on: f<sub>PCLK</sub>=f<sub>HCLK</sub>.

## 7.7.2 Running mode

Table 36 The program is executed in Flash, and the power consumption in running mode

| Parameter                         | Condition                               | f <sub>HCLK</sub> | Typ <sup>(1)</sup>                          | Max <sup>(1)</sup>                           |
|-----------------------------------|-----------------------------------------|-------------------|---------------------------------------------|----------------------------------------------|
|                                   |                                         |                   | T <sub>A</sub> =25°C, V <sub>DD</sub> =3.3V | T <sub>A</sub> =105°C, V <sub>DD</sub> =5.5V |
|                                   |                                         |                   | I <sub>DD</sub> (mA)                        | I <sub>DD</sub> (mA)                         |
| Power consumption in running mode | HSECLK bypass, enabling all peripherals | 64MHz             | 5.29                                        | 5.54                                         |
|                                   |                                         | 32MHz             | 3.33                                        | 3.54                                         |
|                                   |                                         | 16MHz             | 2.61                                        | 2.83                                         |
|                                   |                                         | 8MHz              | 1.91                                        | 2.07                                         |
|                                   | HSECLK bypass, turn off all peripherals | 64MHz             | 3.53                                        | 3.75                                         |
|                                   |                                         | 32MHz             | 2.41                                        | 2.57                                         |
|                                   |                                         | 16MHz             | 2.15                                        | 2.28                                         |
|                                   |                                         | 8MHz              | 1.59                                        | 1.74                                         |

Note: (1) It is tested in comprehensive evaluation instead of in production.

Table 37 Power Consumption in Sleep mode when the program is executed in Flash

| Parameter                       | Condition                               | f <sub>HCLK</sub> | Typ <sup>(1)</sup>                          | Max <sup>(1)</sup>                           |
|---------------------------------|-----------------------------------------|-------------------|---------------------------------------------|----------------------------------------------|
|                                 |                                         |                   | T <sub>A</sub> =25°C, V <sub>DD</sub> =3.3V | T <sub>A</sub> =105°C, V <sub>DD</sub> =5.5V |
|                                 |                                         |                   | I <sub>DD</sub> (mA)                        | I <sub>DD</sub> (mA)                         |
| Power consumption in sleep mode | HSECLK bypass, enabling all peripherals | 64MHz             | 2.63                                        | 2.64                                         |
|                                 |                                         | 32MHz             | 2.36                                        | 2.53                                         |
|                                 |                                         | 16MHz             | 1.79                                        | 1.93                                         |
|                                 |                                         | 8MHz              | 1.48                                        | 1.63                                         |
|                                 | HSECLK bypass, turn off all peripherals | 64MHz             | 1.78                                        | 1.92                                         |
|                                 |                                         | 32MHz             | 1.46                                        | 1.58                                         |
|                                 |                                         | 16MHz             | 1.28                                        | 1.41                                         |
|                                 |                                         | 8MHz              | 1.20                                        | 1.32                                         |

Notes: (1) It is tested in comprehensive evaluation instead of in production.

Table 38 Power Consumption in stop mode

| Parameter                      | Condition       |                                                                                            | Typ <sup>(1)</sup> , (T <sub>A</sub> =25°C) |                       |                       | Max <sup>(1)</sup> , (T <sub>A</sub> =105°C) | Unit |
|--------------------------------|-----------------|--------------------------------------------------------------------------------------------|---------------------------------------------|-----------------------|-----------------------|----------------------------------------------|------|
|                                |                 |                                                                                            | V <sub>DD</sub> =1.8V                       | V <sub>DD</sub> =3.3V | V <sub>DD</sub> =5.5V | V <sub>DD</sub> =5.5V                        |      |
| Power Consumption in stop mode | V <sub>DD</sub> | The kernel and most peripheral devices stop running, while IO, SRAM, and registers remain. | 3.5                                         | 3.7                   | 4.0                   | 20.0                                         | μA   |

| Parameter                         | Condition                | Typ <sup>(1)</sup> , (T <sub>A</sub> =25°C) |                       |                       | Max <sup>(1)</sup> , (T <sub>A</sub> =105°C) | Unit |
|-----------------------------------|--------------------------|---------------------------------------------|-----------------------|-----------------------|----------------------------------------------|------|
|                                   |                          | V <sub>DD</sub> =1.8V                       | V <sub>DD</sub> =3.3V | V <sub>DD</sub> =5.5V | V <sub>DD</sub> =5.5V                        |      |
| Power Consumption in standby mode | 1.5V power is turned off | 1.7                                         | 1.8                   | 2.0                   | 5.0                                          |      |

Notes: (1) It is tested in comprehensive evaluation instead of in production.

## 7.8 Wake-up Time in Low Power Mode

The measurement of wake-up time with low power consumption is from the start of wake-up event to the time when the user program reads the first instruction.

Table 39 Low Power Wake-up Time

| Symbol                 | Parameter                 | Condition           | Min <sup>(1)</sup> | Typ <sup>(1)</sup> (T <sub>A</sub> =25°C) | Max <sup>(1)</sup> | Unit |
|------------------------|---------------------------|---------------------|--------------------|-------------------------------------------|--------------------|------|
| t <sub>WUSLEEP</sub>   | Wake up from sleep mode   | V <sub>DD</sub> =5V | -                  | 1                                         | -                  | μs   |
| t <sub>WUSTOP</sub>    | Wake up from stop mode    |                     | -                  | -                                         | 20                 |      |
| t <sub>WUSTANDBY</sub> | Wake up from standby mode |                     | -                  | -                                         | 1000               |      |

Note: (1) It is tested in comprehensive evaluation instead of in production.

## 7.9 I/O Port Characteristics

Table 40 DC Characteristics (T<sub>A</sub>=-40°C-105°C)

| Symbol           | Parameter                            | Condition                                            | Min                | Typ                 | Max                | Unit |
|------------------|--------------------------------------|------------------------------------------------------|--------------------|---------------------|--------------------|------|
| V <sub>IL</sub>  | Input low level voltage              | V <sub>DD</sub> =5V                                  | -                  | -                   | 0.3V <sub>DD</sub> | V    |
| V <sub>IH</sub>  | Input high level voltage             | V <sub>DD</sub> =5V                                  | 0.7V <sub>DD</sub> | -                   | -                  | V    |
| V <sub>hys</sub> | Schmitt trigger hysteresis           | V <sub>DD</sub> =5V                                  | -                  | 0.07V <sub>DD</sub> | -                  | mV   |
| I <sub>lkg</sub> | Input leakage current                | V <sub>SS</sub> ≤V <sub>IN</sub> ≤V <sub>DDIOx</sub> | -                  | -                   | 1                  | μA   |
| R <sub>PJ</sub>  | Weak pull-up equivalent resistance   | V <sub>IN</sub> =V <sub>SS</sub>                     | 30                 | 40                  | 50                 | kΩ   |
| R <sub>PD</sub>  | Weak pull-down equivalent resistance | V <sub>IN</sub> =V <sub>DDIOx</sub>                  | 30                 | 40                  | 50                 | kΩ   |

Table 41 AC Characteristics (T<sub>A</sub> =25°C)

| Symbol                  | Parameter                                  | Condition                                       | Min | Typ | Max | Unit |
|-------------------------|--------------------------------------------|-------------------------------------------------|-----|-----|-----|------|
| f <sub>max(IO)out</sub> | Maximum frequency                          | C <sub>L</sub> =25pF, V <sub>DD</sub> =2.7~5.5V | -   | -   | 20  | MHz  |
| t <sub>f(IO)out</sub>   | Output falling time from high to low level |                                                 | -   | -   | 15  | ns   |
| t <sub>r(IO)out</sub>   | Output rising time from low to high level  |                                                 | -   | -   | 15  |      |

Figure 23 Definition of Input and Output AC characteristics

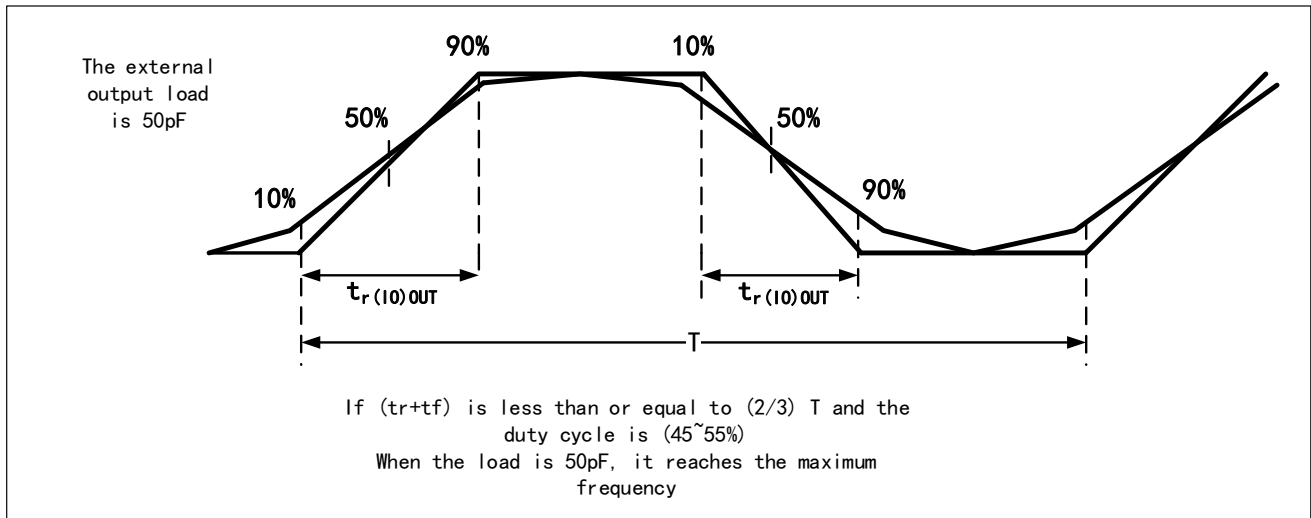


Table 42 Output Drive Current Characteristics ( $T_A = 25^\circ\text{C}$ )

| Symbol   | Parameter                    | Condition                                         | Min          | Typ | Max | Unit |
|----------|------------------------------|---------------------------------------------------|--------------|-----|-----|------|
| $V_{OL}$ | I/O pin outputs low voltage  | $ I_{OLH} =3\text{mA}$ , $V_{DD}\geq 4.5\text{V}$ | -            | -   | 0.4 | V    |
| $V_{OH}$ | I/O pin outputs high voltage | $ I_{OLH} =2\text{mA}$ , $V_{DD}\geq 2.7\text{V}$ | $V_{DD}-0.4$ | -   | -   |      |
| $V_{OL}$ | I/O pin outputs low voltage  | $ I_{OLH} =6\text{mA}$ , $V_{DD}\geq 4.5\text{V}$ | -            | -   | 0.4 |      |
| $V_{OH}$ | I/O pin outputs high voltage | $ I_{OLH} =4\text{mA}$ , $V_{DD}\geq 2.7\text{V}$ | $V_{DD}-0.4$ | -   | -   |      |

Note: It is tested in comprehensive evaluation instead of in production.

## 7.10 NRST pin characteristics

The input drive of NRST pin adopts CMOS process, which is connected with a permanent pull-up resistor  $R_{PU}$

Table 43 NRST Pin Characteristics ( $T_A = -40\sim 105^\circ\text{C}$ )

| Symbol                 | Parameter                                  | Condition          | Min         | Typ          | Max         | Unit       |
|------------------------|--------------------------------------------|--------------------|-------------|--------------|-------------|------------|
| $V_{IL}(\text{NRST})$  | NRST input low voltage                     | $V_{DD}=5\text{V}$ | -           | -            | $0.3V_{DD}$ | V          |
| $V_{IH}(\text{NRST})$  | NRST input high voltage                    | $V_{DD}=5\text{V}$ | $0.7V_{DD}$ | -            | -           |            |
| $V_{hys}(\text{NRST})$ | Voltage hysteresis of NRST Schmitt trigger | $V_{DD}=5\text{V}$ | -           | $0.07V_{DD}$ | -           | mV         |
| $R_{PU}$               | Weak pull-up equivalent resistance         | $V_{IN}=V_{SS}$    | 30          | 40           | 50          | k $\Omega$ |

## 7.11 Communication Interface

### 7.11.1 I2C Interface Characteristics

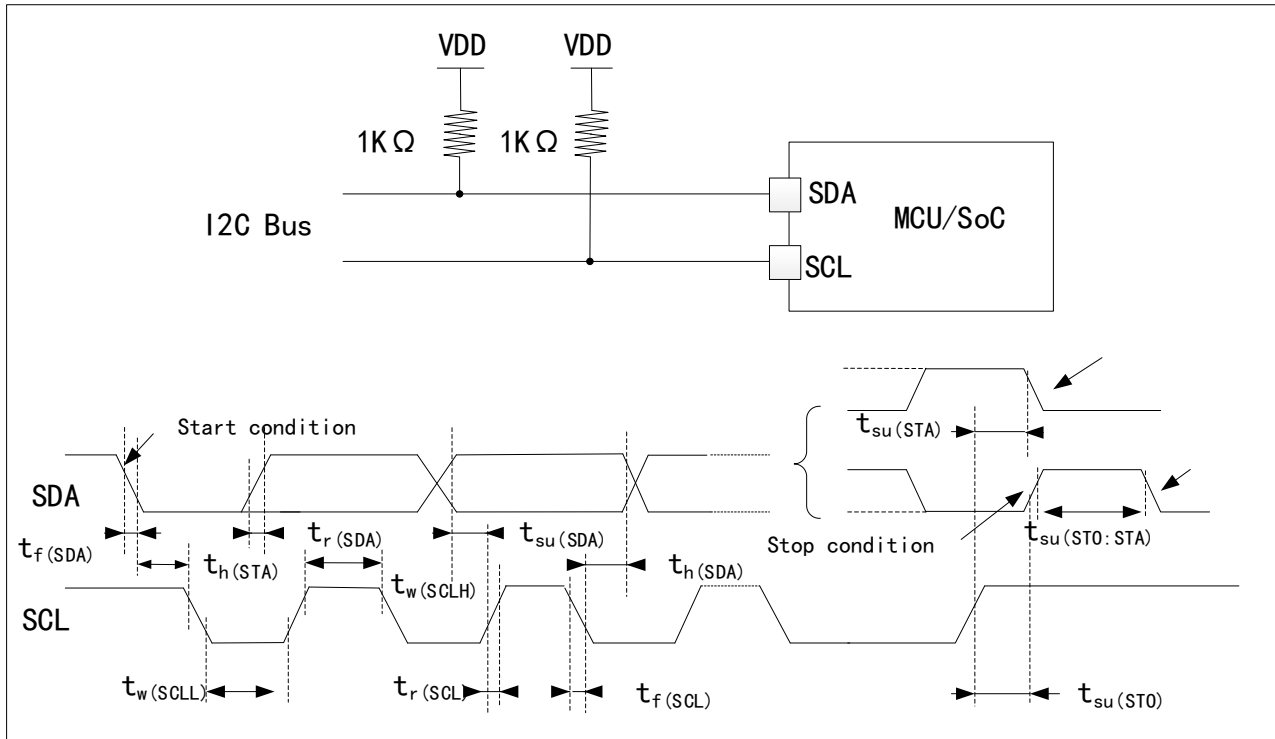
- Standard mode (Sm): Up to 100kbit/s
- Fast mode (Fm): Up to 400kbit/s
- Ultrafast mode (Fm+): Up to 1Mbit/s

Table 44 I2C Interface Characteristics ( $T_A=25^{\circ}\text{C}$ ,  $V_{DD}=3.3\text{V}$ )

| Symbol                  | Parameter                                              | Standard I2C |        | Fast I2C |        | Ultrafast I2C |        | Unit          |
|-------------------------|--------------------------------------------------------|--------------|--------|----------|--------|---------------|--------|---------------|
|                         |                                                        | Min          | Max    | Min      | Max    | Min           | Max    |               |
| $t_{w(\text{SCL})}$     | SCL clock low time                                     | -            | 5.00   | 1.65     | 1.66   | 656.85        | 658.62 | $\mu\text{s}$ |
| $t_{w(\text{SCLH})}$    | SCL clock high time                                    | -            | 4.96   | 789.35   | 790.49 | 290.91        | 292.17 |               |
| $t_{su(\text{SDA})}$    | SDA setup time                                         | -            | 4.56   | 1.21     | 1.22   | 217.66        | 219.54 | ns            |
| $t_h(\text{SDA})$       | SDA data holding time                                  | 85.88        | 406.20 | 85.81    | 405.99 | 85.53         | 404.93 |               |
| $t_r(\text{SDA})$       | SDA rising time                                        | 30.24        | 31.63  | 30.96    | 31.53  | 30.32         | 31.45  |               |
| $t_r(\text{SCL})$       | SCL rising time                                        | 30.64        | 32.28  | 31.10    | 31.45  | 31.14         | 31.45  |               |
| $t_f(\text{SDA})$       | SDA falling time                                       | 2.66         | 4.59   | 2.58     | 4.81   | 4.66          | 4.79   |               |
| $t_f(\text{SCL})$       | SCL falling time                                       | 5.18         | 5.40   | 5.28     | 5.40   | 5.34          | 5.50   |               |
| $t_h(\text{STA})$       | Start condition holding time                           | 5.05         | 5.06   | 884.35   | 886.09 | 385.07        | 385.84 | $\mu\text{s}$ |
| $t_{su(\text{STA})}$    | Repeated start condition setup time                    | -            | 4.98   | 805.40   | 806.12 | 306.93        | 308.20 |               |
| $t_{su(\text{STO})}$    | Setup time of stop condition                           | -            | 9.99   | 2.46     | 2.47   | 969.51        | 970.96 | $\mu\text{s}$ |
| $t_{w(\text{STO:STA})}$ | Time from stop condition to start condition (bus idle) | 711.81       | 713.14 | 398.95   | 399.40 | 570.44        | 572.58 | $\mu\text{s}$ |
| $t_{AF}$                | Analog filter width                                    | -            | -      | 50       | -      | -             | 260    | ns            |

Note: It is tested in comprehensive evaluation instead of in production.

Figure 24 Bus AC Waveform and Measurement Circuit



Note: the measuring points are set at CMOS levels:  $0.3V_{DD}$  and  $0.7V_{DD}$ .

## 7.11.2 SPI Interface Characteristics

Table 45 SPI Characteristics ( $T_A=25^{\circ}\text{C}$ ,  $V_{DD}=3.3\text{V}$ )

| Symbol                                                   | Parameter                     | Condition                                                                                 | Min                     | Typ | Max | Unit |
|----------------------------------------------------------|-------------------------------|-------------------------------------------------------------------------------------------|-------------------------|-----|-----|------|
| $f_{\text{SCK}}$<br>$1/t_{\text{c}}(\text{SCK})$         | SPI clock frequency           | Master mode                                                                               | -                       | -   | 16  | MHz  |
|                                                          |                               | Slave mode                                                                                | -                       | -   | 20  |      |
| $t_{\text{r}}(\text{SCK})$                               | SPI clock rising time         | Load capacitance: $C=15\text{pF}$                                                         | 2                       | -   | 7   | ns   |
| $t_{\text{f}}(\text{SCK})$                               | SPI clock falling time        |                                                                                           | 2                       | -   | 8   | ns   |
| $t_{\text{su}}(\text{NSS})$                              | NSS setup time                | Slave mode                                                                                | $4T_{\text{PCLK}}$      | -   | -   | ns   |
| $t_{\text{h}}(\text{NSS})$                               | NSS hold time                 | Slave mode                                                                                | $2T_{\text{PCLK}} + 10$ | -   | -   | ns   |
| $t_{\text{w}}(\text{SCKH})$                              | SCK high time                 | Master mode, $f_{\text{PCLK}} = 32\text{ MHz}$ ,<br>preassigned frequency coefficient = 4 | 21                      | -   | 32  | ns   |
| $t_{\text{w}}(\text{SCKL})$                              | SCK low time                  |                                                                                           | 25                      | -   | 33  | ns   |
| $t_{\text{su}}(\text{MI})$<br>$t_{\text{su}}(\text{SI})$ | Data input setup time         | Master mode                                                                               | 2                       | -   | -   | ns   |
|                                                          |                               | Slave mode                                                                                | 2                       | -   | -   |      |
| $t_{\text{h}}(\text{MI})$<br>$t_{\text{h}}(\text{SI})$   | Data input hold time          | Master mode                                                                               | 2                       | -   | -   | ns   |
|                                                          |                               | Slave mode                                                                                | 2                       | -   | -   |      |
| $t_{\text{a}}(\text{SO})$                                | Data output access time       | Slave mode, $f_{\text{PCLK}}=20\text{MHz}$                                                | -                       | -   | 15  | ns   |
| $t_{\text{dis}}(\text{SO})$                              | Data output disable time      | Slave mode                                                                                | -                       | -   | 18  | ns   |
| $t_{\text{v}}(\text{SO})$                                | Effective time of data output | Slave mode (after enable edge)                                                            | 12                      | -   | 25  | ns   |
| $t_{\text{v}}(\text{MO})$                                |                               | Master mode (after enable edge)                                                           | 16                      | -   | 34  | ns   |
| $t_{\text{h}}(\text{SO})$                                | Data output holding time      | Slave mode (after enable edge)                                                            | 11                      | -   | 16  | ns   |
| $t_{\text{h}}(\text{MO})$                                |                               | Master mode (after enable edge)                                                           | 14                      | -   | 28  |      |

Note: It is tested in comprehensive evaluation instead of in production.

Figure 25 SPI Timing Diagram—Slave Mode and CPHA=0

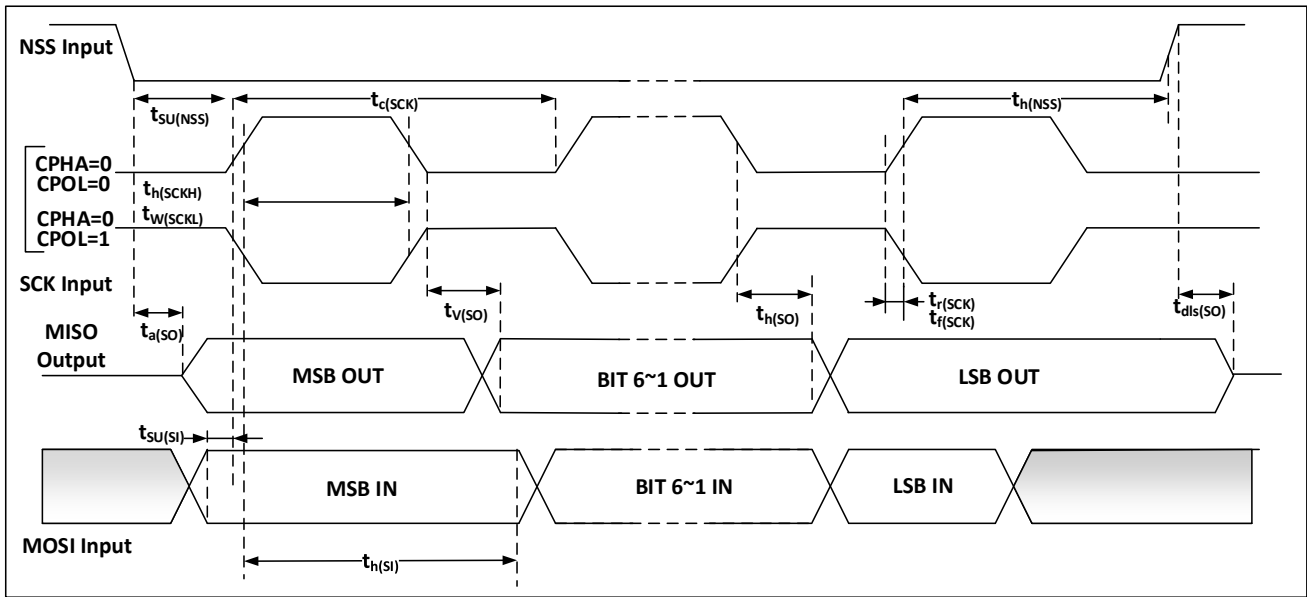
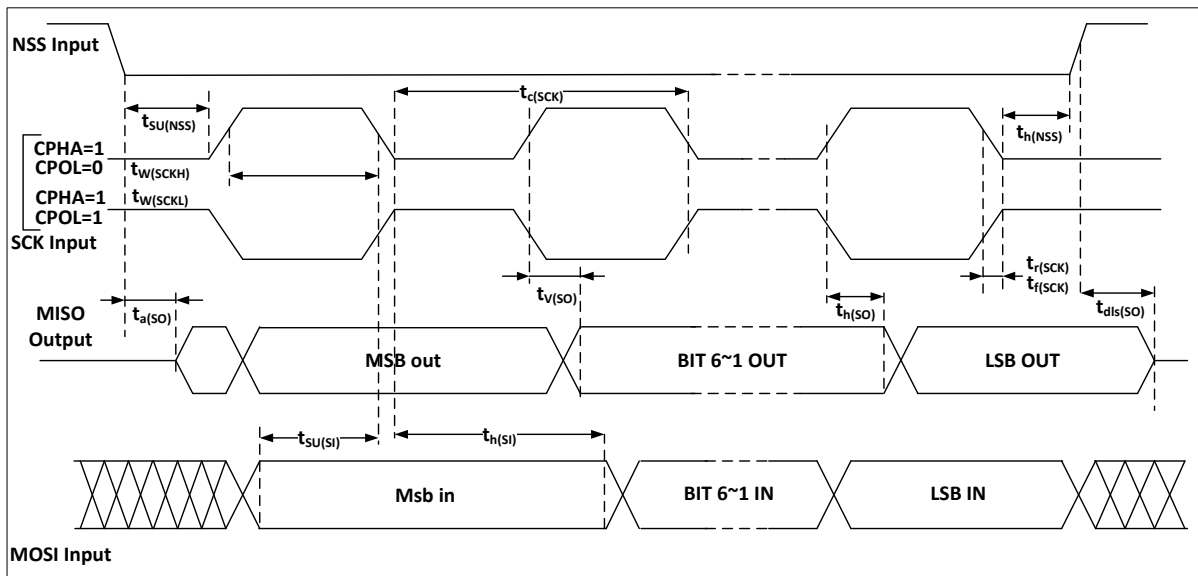
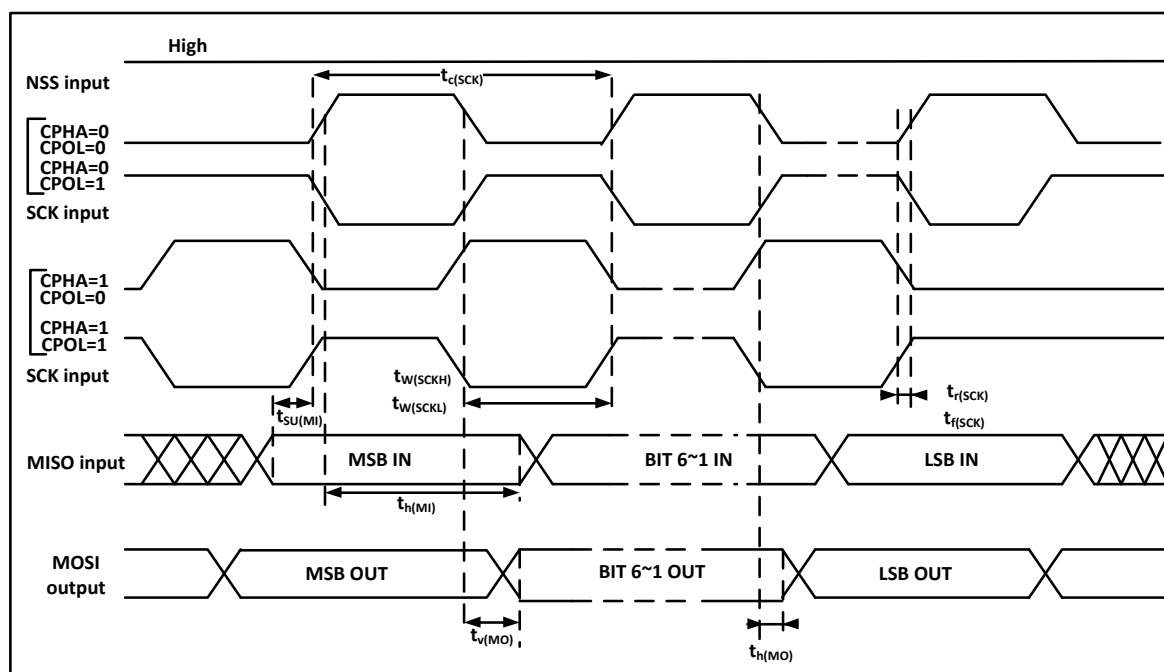


Figure 26 SPI Timing Diagram —Slave Mode and CPHA=1



Note: the measuring points are set at CMOS levels: 0.3V<sub>DD</sub> and 0.7V<sub>DD</sub>.

Figure 27 SPI Timing Diagram—Master mode



Note: the measuring points are set at CMOS levels:  $0.3V_{DD}$  and  $0.7V_{DD}$ .

## 7.12 ADC

### 7.12.1 12-bit ADC Characteristics

Table 46 12-bit ADC Characteristics

| Symbol    | Parameter          | Condition         | Min  | Typ | Max    | Unit |
|-----------|--------------------|-------------------|------|-----|--------|------|
| $V_{DDA}$ | Supply voltage     | standard voltage  | 2.7  | -   | 5.5    | V    |
|           |                    | low voltage       | 2    | -   | 2.7    | V    |
|           |                    | extra low voltage | 1.75 | -   | 2      | V    |
| $F_{REQ}$ | Clock frequency    | standard voltage  | -    | -   | 32     | MHz  |
|           |                    | low voltage       | -    | -   | 16     | MHz  |
|           |                    | extra low voltage | -    | -   | 16     | MHz  |
| REF       | Reference source   | standard voltage  | 2.4  | -   | 5.5    | V    |
|           |                    | low voltage       | 2    | -   | 2.4    | V    |
|           |                    | extra low voltage | -    | 1.1 | -      | V    |
| $V_{AIN}$ | Input range        | standard voltage  | 20   | -   | REF-20 | mV   |
|           |                    | low voltage       | 20   | -   | REF-20 | mV   |
|           |                    | extra low voltage | 20   | -   | 1080   | mV   |
| ENOB      | Effective accuracy | standard voltage  | -    | 10  | -      | BIT  |
|           |                    | low voltage       | -    | 9   | -      | BIT  |

| Symbol            | Parameter          | Condition                     | Min   | Typ   | Max  | Unit |
|-------------------|--------------------|-------------------------------|-------|-------|------|------|
|                   |                    | extra low voltage             | -     | 8     | -    | BIT  |
| I <sub>DD</sub>   | Power dissipation  | standard voltage              | -     | 0.95  | 1.15 | mA   |
|                   |                    | standard voltage<br>low power | -     | 0.68  | 0.84 | mA   |
|                   |                    | low voltage                   | -     | 0.58  | 0.73 | mA   |
|                   |                    | extra low voltage             | -     | 0.74  | 0.98 | mA   |
| PD                | Electric leakage   | standard voltage              | -     | 30    | 9200 | nA   |
| R <sub>ADC</sub>  | Input resistance   | NA                            | -     | -     | 1000 | Ω    |
| C <sub>ADC</sub>  | Sampling capacitor | NA                            | -     | 1     | -    | pF   |
| F <sub>s</sub>    | Sampling rate      | NA                            | 0.119 | 1.778 | 2    | MHz  |
| T <sub>s</sub>    | Sampling time      | NA                            | 31.25 | 93.75 | 7969 | ns   |
| T <sub>CONV</sub> | Conversion time    | NA                            | 16    | 18    | 270  | T    |
| T <sub>SU</sub>   | Start-up time      | NA                            | -     | -     | 2    | μs   |

Note: It is tested in comprehensive evaluation instead of in production.

Table 47 Accuracy of 12-bit ADC

| Symbol         | Parameter                 | Condition         | Min | Typ  | Max  | Unit |
|----------------|---------------------------|-------------------|-----|------|------|------|
| E <sub>T</sub> | Composite error           | standard voltage  | 0   | ±2.1 | ±3.9 | LSB  |
|                |                           | low voltage       | 0   | ±3.5 | ±5.3 |      |
|                |                           | extra low voltage | 0   | -    | ±80  |      |
| E <sub>O</sub> | Offset error              | standard voltage  | 0   | ±1.5 | ±2.5 |      |
|                |                           | low voltage       | 0   | ±2.5 | ±3.5 |      |
|                |                           | extra low voltage | 0   | ±4.5 | ±6.5 |      |
| E <sub>G</sub> | Gain error                | standard voltage  | 0   | ±1.5 | ±3   |      |
|                |                           | low voltage       | 0   | ±2.5 | ±4   |      |
|                |                           | extra low voltage | 0   | -    | ±80  |      |
| E <sub>D</sub> | Differential linear error | standard voltage  | 0   | ±1   | ±1.5 |      |
|                |                           | low voltage       | 0   | ±2   | ±2.5 |      |
|                |                           | extra low voltage | 0   | ±3   | ±3.5 |      |
| E <sub>L</sub> | Integral linearity error  | standard voltage  | 0   | ±1.5 | ±2   |      |
|                |                           | low voltage       | 0   | ±2.5 | ±3   |      |
|                |                           | extra low voltage | 0   | ±3.5 | ±4   |      |

Note: It is tested in comprehensive evaluation instead of in production.

## 7.12.2 Temperature Sensor Characteristics

Table 48 Temperature Sensor Characteristics

| Symbol  | Parameter                                                        | Min | Typ     | Max  | Unit            |
|---------|------------------------------------------------------------------|-----|---------|------|-----------------|
| Slope   | Average slope( $V_{DD} = 5.5V$ , $T_A = -40 \sim 105^{\circ}C$ ) | -   | -3.802  | -    | mV/ $^{\circ}C$ |
| V25     | Voltage at $25^{\circ}C$                                         | -   | 1.36    | -    | V               |
| Ts_temp | Sampling time of the ADC when reading the temperature            | -   | -       | 17.1 | $\mu s$         |
| TL      | temperature departure                                            | -   | $\pm 5$ | -    | $^{\circ}C$     |

## 7.13 Comparator

Table 49 Comparator Characteristics

| Symbol       | Parameter                                                                                    | Condition                                       | Min | Typ      | Max       | Unit    |
|--------------|----------------------------------------------------------------------------------------------|-------------------------------------------------|-----|----------|-----------|---------|
| $V_{DDA}$    | Analog supply voltage                                                                        | -                                               | 2.7 | 5        | 5.5       | V       |
| $V_{IN}$     | Comparator input voltage range                                                               | -                                               | 0   | -        | $V_{DDA}$ | -       |
| $V_{OUT}$    | Comparator output voltage range                                                              | -                                               | 0   | -        | $V_{DDA}$ | V       |
| $t_D$        | propagation delay(The time it takes for the input flip to change to 50% of the output flip.) | -                                               | -   | 150      | 200       | ns      |
| -            | Operating current                                                                            | $T_A = -40 \sim 105^{\circ}C$ / $V_{DD} = 5.5V$ | -   | 350      | 450       | $\mu A$ |
| $V_{OFFSET}$ | Offset voltage                                                                               | -                                               | -10 | -        | 10        | mV      |
| $V_{hys}$    | Hysteresis voltage                                                                           | Hysteresis voltage control bit                  | 00  | 0        | -         | mV      |
|              |                                                                                              |                                                 | 01  | $\pm 20$ |           |         |
|              |                                                                                              |                                                 | 10  | $\pm 40$ |           |         |
|              |                                                                                              |                                                 | 11  | $\pm 80$ |           |         |

Note: It is tested in comprehensive evaluation instead of in production.

## 7.14 Operational amplifier

Table 50 Operational amplifier Characteristics

| Symbol           | Parameter                   | Condition  | Min                | Typ | Max               | Unit   |
|------------------|-----------------------------|------------|--------------------|-----|-------------------|--------|
| $V_{DDA}$        | Analog power supply voltage | -          | 2.7                | 5   | 5.5               | V      |
| Closed-loop gain | Gain factor                 | Internal   | 1                  | -   | 16                | factor |
|                  |                             | External   | 1                  | -   | 32                |        |
| CMIR             | Common-mode input range     | -          | $-(V_{DDA}-300)/G$ | -   | $(V_{DDA}-300)/G$ | V      |
| Voffset          | Input offset voltage        | -          | -10                | -   | 10                | mV     |
| IDDOPAMP         | Current consumption         | non-loaded | -                  | 1   | -                 | mA     |

| Symbol              | Parameter                           | Condition                             | Min  | Typ | Max                   | Unit |
|---------------------|-------------------------------------|---------------------------------------|------|-----|-----------------------|------|
| SR                  | Slew rate                           | CL=15pF, RL≥4KΩ, G=1                  | -    | 14  | -                     | V/μs |
| T <sub>wakeup</sub> | Setup time from shutdown to wake-up | CL≤15pF, RL≥4KΩ, Internal gain G=1~16 | -    | 1   | 2                     | μs   |
|                     |                                     | CL≤15pF, RL≥4KΩ, External gain G=1~32 | -    | 2   | 3                     |      |
| VOHSAT              | High saturation output voltage      | CL≤15pF, RL=4KΩ                       | -    | -   | V <sub>DDA</sub> -100 | mV   |
| VOLSAT              | Low saturation output voltage       |                                       | 100  | -   | -                     | mV   |
| -                   | Gain accuracy error                 |                                       | -2.5 | -   | 2.5                   | %    |

Note: It is tested in comprehensive evaluation instead of in production.

## 7.15 Gate driver for M3114

### 7.15.1 General Working Conditions

T<sub>A</sub>=25°C, all pins take GND as the reference points, unless otherwise specified.

Table 51 General Operating Conditions

| Symbol               | Parameter                                  | Min                    | Typ                     | Max                     | Unit |
|----------------------|--------------------------------------------|------------------------|-------------------------|-------------------------|------|
| T <sub>A</sub>       | Ambient temperature                        | -40                    | -                       | 105                     | °C   |
| V <sub>HO1,2,3</sub> | High-side output voltage                   | V <sub>S1,2,3</sub>    | V <sub>S1,2,3</sub> +15 | V <sub>B1,2,3</sub>     | V    |
| V <sub>LO1,2,3</sub> | Low-side output voltage                    | 0                      | 15                      | VCC                     | V    |
| V <sub>B1,2,3</sub>  | High-side floating offset absolute voltage | V <sub>S1,2,3</sub> +5 | V <sub>S1,2,3</sub> +15 | V <sub>S1,2,3</sub> +20 | V    |
| V <sub>S1,2,3</sub>  | High-side floating offset relative voltage | GND-5                  | -                       | 140                     | V    |
| VCC                  | Supply voltage                             | 5                      | 15                      | 20                      | V    |
| V <sub>IN</sub>      | Input voltage (HIN1, 2, 3/LIN1, 2, 3)      | 0                      | -                       | 5                       | V    |
| VG                   | LDO switch enable pin                      | 0                      | -                       | 5                       | V    |
| PGND                 | Power ground                               | -1.0                   | 0                       | 1.0                     | V    |

Note:

- (1) When V<sub>B1,2,3</sub>=V<sub>S1,2,3</sub>+10, and V<sub>S1,2,3</sub> is (COM-5V)~(COM-VBS), the HO logic state is maintained. When V<sub>S1,2,3</sub> is (COM-5V) ~140V, HO operates normally.
- (2) Operation beyond the recommended conditions for a long time may affect its reliability.

### 7.15.2 Electrical characteristic

T<sub>A</sub>=25°C, VCC=VBS<sub>1,2,3</sub>=15V, VS<sub>1,2,3</sub>=GND; all pins take GND as the reference points, unless otherwise specified.

Table 52 Supply Voltage Parameters

| Symbol             | Parameter                             | Min | Typ | Max | Unit |
|--------------------|---------------------------------------|-----|-----|-----|------|
| VBS <sub>HY+</sub> | VBS undervoltage high-level potential | 4.0 | 4.3 | 4.6 | V    |
| VBS <sub>HY-</sub> | VBS undervoltage low-level potential  | 3.7 | 4.0 | 4.3 | V    |

|                    |                                       |      |      |      |   |
|--------------------|---------------------------------------|------|------|------|---|
| VBS <sub>HY</sub>  | VBS undervoltage hysteresis level     | 0.2  | 0.3  | 0.4  | V |
| VCC <sub>HY+</sub> | VCC undervoltage high-level potential | 4.5  | 4.6  | 4.75 | V |
| VCC <sub>HY-</sub> | VCC undervoltage low-level potential  | 4.25 | 4.35 | 4.45 | V |
| VCC <sub>HY</sub>  | VCC undervoltage hysteresis level     | 0.15 | 0.25 | 0.3  | V |

Table 53 Supply Current Parameters

| Symbol           | Parameter                                | Condition                    | Min | Typ  | Max  | Unit |
|------------------|------------------------------------------|------------------------------|-----|------|------|------|
| I <sub>CCD</sub> | VCC dynamic current                      | f <sub>LIN1,2,3</sub> =20kHz | 700 | 1350 | 2000 | uA   |
| I <sub>BSD</sub> | VBS dynamic current                      | f <sub>HIN1,2,3</sub> =20kHz | 100 | 150  | 400  | uA   |
| I <sub>CCQ</sub> | VCC quiescent current                    | V <sub>IN</sub> =0V          | 700 | 950  | 1200 | uA   |
| I <sub>BSQ</sub> | VBS quiescent current                    | V <sub>HIN</sub> =0V         | 30  | 50   | 80   | uA   |
| I <sub>LK</sub>  | VB floating power supply leakage current | VB=225V                      | 0   | 0.1  | 5    | uA   |

Table 54 Time Parameters

| Symbol           | Parameter                             | Condition             | Min | Typ | Max | Unit |
|------------------|---------------------------------------|-----------------------|-----|-----|-----|------|
| t <sub>ON</sub>  | Output rising edge transmission time  | No Load               | 160 | 270 | 350 | ns   |
| t <sub>OFF</sub> | Output falling edge transmission time | No Load               | 160 | 270 | 350 | ns   |
| t <sub>r</sub>   | Output rise time                      | C <sub>L</sub> =3.3nF | 55  | 90  | 110 | ns   |
| t <sub>f</sub>   | Output fall time                      | C <sub>L</sub> =3.3nF | 40  | 60  | 90  | ns   |
| DT               | Dead time                             | No Load               | 300 | 500 | 650 | ns   |
| MT               | High and low-side matching time       | No Load               | 0   | 20  | 50  | ns   |
| tLDO_ON          | LDO enable transmission time          | -                     | 300 | 400 | 700 | ns   |
| tLDO_OFF         | LDO disable transmission time         | -                     | 300 | 400 | 700 | ns   |

Table 55 Input-end Parameters

| Symbol            | Parameter                  | Condition           | Min  | Typ  | Max  | Unit |
|-------------------|----------------------------|---------------------|------|------|------|------|
| V <sub>IN+</sub>  | Input high-level potential | -                   | 1.70 | 2.15 | 2.40 | V    |
| V <sub>IN-</sub>  | Input low-level potential  | -                   | 0.65 | 1.45 | 1.85 | V    |
| I <sub>IN+</sub>  | Input high-level current   | V <sub>IN</sub> =5V | 8    | 11   | 15   | uA   |
| I <sub>IN-</sub>  | Input low-level current    | V <sub>IN</sub> =0V | -1   | 0    | 1    | uA   |
| V <sub>INHY</sub> | Input hysteresis level     | -                   | 0.45 | 0.7  | 1.1  | V    |

Table 56 Driver output-end Parameters

| Symbol            | Parameter                 | Condition                                        | Min | Typ  | Max | Unit |
|-------------------|---------------------------|--------------------------------------------------|-----|------|-----|------|
| V <sub>OUT+</sub> | High-level output voltage | I <sub>OUT</sub> =100mA<br>15V- V <sub>OUT</sub> | -   | 0.51 | -   | V    |
| V <sub>OUT-</sub> | Low-level output voltage  | I <sub>OUT</sub> =100mA                          | -   | 0.18 | -   | V    |

| Symbol     | Parameter                              | Condition                                     | Min  | Typ  | Max  | Unit |
|------------|----------------------------------------|-----------------------------------------------|------|------|------|------|
|            |                                        | $V_{OUT}-GND$                                 |      |      |      |      |
| $V_{OUT-}$ | Low-level output voltage               | $I_{OUT}=10mA$<br>$15V- V_{OUT}$              | 0.05 | 0.07 | 0.1  | V    |
| $V_{OUT-}$ | Low-level output voltage               | $I_{OUT}=10mA$<br>$V_{OUT}-GND$               | 0.02 | 0.04 | 0.08 | V    |
| $I_{OUT+}$ | High-level short-circuit pulse current | $V_{IN}=5V$<br>$V_O=0V$<br>$PWD\leq 10\mu s$  | 0.7  | 0.9  | 1.2  | A    |
| $I_{OUT-}$ | Low-level short-circuit pulse current  | $V_{IN}=0V$<br>$V_O=15V$<br>$PWD\leq 10\mu s$ | 0.9  | 1.1  | 1.5  | A    |

Table 57 Built-in LDO parameters

| Parameter              | Symbol                                | Condition                                           | Min  | Typ | Max  | Unit        |
|------------------------|---------------------------------------|-----------------------------------------------------|------|-----|------|-------------|
| $V_{LDO}$              | LDO output voltage                    | $VCC=5\sim 20V$ , $I_{load}=1mA\sim 60mA$           | 3.23 | 3.3 | 3.37 | V           |
| $\Delta V_{LDO\_LOAD}$ | Load adjustment                       | $VCC=15V$ , $I_{load}=0.1mA\sim 33mA$               | -    | 20  | 40   | mV          |
| $\Delta V_{LDO\_LOAD}$ | Load adjustment                       | $VCC=5V$ , $I_{load}=0.1mA\sim 33mA$                | -    | 30  | 60   | mV          |
| $\Delta V_{LDO\_VCC}$  | Power adjustment                      | $VCC=4\sim 20V$ , $I_{load}=0.1mA$                  | -    | 10  | 20   | mV          |
| $\Delta V_{LDO\_VCC}$  | Power adjustment                      | $VCC=4\sim 20V$ , $I_{load}=33mA$                   | -    | 15  | 30   | mV          |
| PSR                    | Power suppression                     | $F_{eq}=10kHz$ , $VCC=15V$ ,<br>$CL=10\mu F$        | 50   | 60  | -    | dB          |
| $\Delta V_{LDO\_TEMP}$ | Temperature drift                     | $I_{load}=1mA$ ,<br>$-40^{\circ}C\sim 105^{\circ}C$ | -    | 50  | 100  | mV          |
| $I_{INIT\_LIMIT}$      | Output startup current limiting       | $V_{out}<0.7V$                                      | 15   | 25  | 40   | mA          |
| $I_{OUT\_LIMIT}$       | Maximum output current limiting       | $VCC=15V$                                           | 70   | 100 | 130  | mA          |
| $OTP_{HY+}$            | High temperature protection threshold | $VCC=15V$                                           | 147  | 151 | 157  | $^{\circ}C$ |
| $OTP_{HY-}$            | Low temperature protection threshold  | $VCC=15V$                                           | 120  | 125 | 131  | $^{\circ}C$ |
| $OTP_{HY}$             | Temperature protection hysteresis     | $VCC=15V$                                           | 21   | 27  | 33   | $^{\circ}C$ |
| $C_{load}$             | Load capacitance                      | -                                                   | 4.7  | 10  | 100  | $\mu F$     |
| ESR                    | Equivalent series resistance          | -                                                   | 0    | 0   | 1    | $\Omega$    |

## 7.16 Gate driver for M3115

### 7.16.1 General Working Conditions

Unless otherwise specified,  $T_A=25^{\circ}\text{C}$ ,  $V_{CC}=V_{BS1,2,3}=15\text{V}$ ,  $V_{S1,2,3}=\text{GND}$ , and all pins take GND as the reference point.

Table 58 General Operating Conditions

| Symbol        | Parameter                                  | Min              | Typ             | Max             | Unit               |
|---------------|--------------------------------------------|------------------|-----------------|-----------------|--------------------|
| $T_A$         | Ambient temperature                        | -40              | -               | 105             | $^{\circ}\text{C}$ |
| $V_{HO1,2,3}$ | High-side output voltage                   | $V_{S1,2,3}$     | $V_{S1,2,3}+15$ | $V_{B1,2,3}$    | V                  |
| $V_{LO1,2,3}$ | Low-side output voltage                    | 0                | 15              | VCC             | V                  |
| $V_{B1,2,3}$  | High-side floating offset absolute voltage | $V_{S1,2,3}+5.5$ | $V_{S1,2,3}+15$ | $V_{S1,2,3}+20$ | V                  |
| $V_{S1,2,3}$  | High-side floating offset relative voltage | -5               | -               | 140             | V                  |
| VCC           | Supply voltage                             | 5.5              | 15              | 20              | V                  |
| $V_{IN}$      | Input voltage (HIN1, 2, 3/LIN1, 2, 3)      | 0                | -               | 5               | V                  |

Note:

- (1) When  $V_{B1,2,3}=V_{S1,2,3}+10$ , and  $V_{S1,2,3}$  is (COM-5V)~(COM-VBS), the HO logic state is maintained. When  $V_{S1,2,3}$  is (COM-5V) ~140V, HO operates normally.
- (2) Operation beyond the recommended conditions for a long time may affect its reliability.

### 7.16.2 Electrical characteristic

$T_A=25^{\circ}\text{C}$ ,  $V_{CC}=V_{BS1,2,3}=12\text{V}$ ,  $V_{S1,2,3}=\text{GND}$ ; all pins take GND as the reference points, unless otherwise specified.

Table 59 Supply Voltage Parameters

| Symbol         | Parameter                             | Condition | Min | Typ | Max | Unit |
|----------------|---------------------------------------|-----------|-----|-----|-----|------|
| $V_{BS_{HY+}}$ | VBS undervoltage high-level potential | -         | 3.2 | 4.2 | 5.0 | V    |
| $V_{BS_{HY-}}$ | VBS undervoltage low-level potential  | -         | 3.1 | 4.0 | 4.9 | V    |
| $V_{BS_{HY}}$  | VBS undervoltage hysteresis level     | -         | -   | 0.2 | -   | V    |
| $V_{CC_{HY+}}$ | VCC undervoltage high-level potential | -         | 3.5 | 4.5 | 5.4 | V    |
| $V_{CC_{HY-}}$ | VCC undervoltage low-level potential  | -         | 3.4 | 4.3 | 5.2 | V    |
| $V_{CC_{HY}}$  | VCC undervoltage hysteresis level     | -         | -   | 0.2 | -   | V    |
| VSQN           | VS Static negative pressure           | VBS=15V   | -5  | -   | -   | V    |

Table 60 Supply Current Parameters

| Symbol    | Parameter             | Condition                                                     | Min | Typ | Max | Unit          |
|-----------|-----------------------|---------------------------------------------------------------|-----|-----|-----|---------------|
| $I_{CCD}$ | VCC dynamic current   | $f_{LIN1,2,3}=20\text{kHz}$                                   | 750 | 820 | 940 | $\mu\text{A}$ |
| $I_{BSD}$ | VBS dynamic current   | $f_{HIN1,2,3}=20\text{kHz}$ ,<br>$I_{BSD1}+I_{BSD2}+I_{BSD3}$ | 310 | 390 | 680 | $\mu\text{A}$ |
| $I_{CCQ}$ | VCC quiescent current | $V_{IN}=0\text{V}$                                            | 290 | 320 | 490 | $\mu\text{A}$ |

|           |                                          |                                          |    |     |     |         |
|-----------|------------------------------------------|------------------------------------------|----|-----|-----|---------|
| $I_{BSQ}$ | VBS quiescent current                    | $V_{HIN}=0V, I_{BSQ1}+I_{BSQ2}+I_{BSQ3}$ | 80 | 110 | 140 | $\mu A$ |
| $I_{LK}$  | VB floating power supply leakage current | $V_{IN}=float, VB=225V$                  | -  | -   | 10  | $\mu A$ |

Table 61 Time Parameters

| Symbol    | Parameter                             | Condition   | Min | Typ | Max | Unit |
|-----------|---------------------------------------|-------------|-----|-----|-----|------|
| $t_{ON}$  | Output rising edge transmission time  | No Load     | 130 | 170 | 250 | ns   |
| $t_{OFF}$ | Output falling edge transmission time | No Load     | 130 | 170 | 250 | ns   |
| $t_r$     | Output rise time                      | $C_L=3.3nF$ | 20  | 35  | 60  | ns   |
| $t_f$     | Output fall time                      | $C_L=3.3nF$ | 15  | 20  | 40  | ns   |
| DT        | Dead time                             | No Load     | 160 | 220 | 300 | ns   |
| MDT       | Dead zone matching time               | No Load     | -   | -   | 30  | ns   |
| MT        | High and low-side matching time       | No Load     | -   | -   | 30  | ns   |

Table 62 Input-end Parameters

| Symbol     | Parameter                  | Condition                    | Min | Typ | Max | Unit    |
|------------|----------------------------|------------------------------|-----|-----|-----|---------|
| $V_{IN+}$  | Input high-level potential | -                            | 1.6 | 2.0 | 2.3 | V       |
| $V_{IN-}$  | Input low-level potential  | -                            | 0.8 | 1.7 | 2.1 | V       |
| $I_{IN+}$  | Input high-level current   | $V_{HIN}=5V$<br>$V_{LIN}=0V$ | 9   | 13  | 19  | $\mu A$ |
| $I_{IN-}$  | Input low-level current    |                              | -1  | 0   | 1   | $\mu A$ |
| $V_{INHY}$ | Input hysteresis level     | -                            | -   | 0.3 | -   | V       |

Table 63 Driver output-end Parameters

| Symbol     | Parameter                              | Condition                              | Min | Typ | Max | Unit |
|------------|----------------------------------------|----------------------------------------|-----|-----|-----|------|
| $V_{OUT+}$ | High-level output voltage              | $I_{OUT}=100mA, 15V- V_{OUT}$          | 220 | 330 | 800 | mV   |
| $V_{OUT-}$ | Low-level output voltage               | $I_{OUT}=100mA, V_{OUT}-GND$           | 80  | 140 | 300 | mV   |
| $V_{OUT-}$ | Low-level output voltage               | $I_{OUT}=20mA, 15V- V_{OUT}$           | 60  | 70  | 150 | mV   |
| $V_{OUT-}$ | Low-level output voltage               | $I_{OUT}=20mA, V_{OUT}-GND$            | 15  | 30  | 60  | mV   |
| $I_{OUT+}$ | High-level short-circuit pulse current | $V_{IN}=5V, V_O=0V, PWD \leq 10\mu s$  | 1.6 | 2.0 | 3.0 | A    |
| $I_{OUT-}$ | Low-level short-circuit pulse current  | $V_{IN}=0V, V_O=15V, PWD \leq 10\mu s$ | 2.0 | 2.7 | 3.2 | A    |

Table 64 Bootloader parameter

| Symbol       | Parameter                  | Condition         | Min | Typ | Max | Unit |
|--------------|----------------------------|-------------------|-----|-----|-----|------|
| $I_{BSD15L}$ | Bootstrap charging current | $VCC=15V, VB=11V$ | 10  | 15  | 25  | mA   |
| $I_{BSD15H}$ | Bootstrap charging current | $VCC=15V, VB=0V$  | 60  | 85  | 110 | mA   |

## 7.17 Gate driver for M3122

### 7.17.1 General Working Conditions

$T_A=25^{\circ}\text{C}$ ; unless otherwise specified, all pins take GND as the reference points.

Table 65 General Operating Conditions

| Symbol            | Parameter                    | Min | Typ | Max | Unit               |
|-------------------|------------------------------|-----|-----|-----|--------------------|
| $V_{\text{SUP1}}$ | 5V supply voltage            | 5.5 | 24  | 30  | V                  |
| $V_{\text{SUP2}}$ | Driving supply voltage       | 5.5 | 24  | 30  | V                  |
| $V_{\text{IN}}$   | Input voltage (HIN/LIN)      | 0   | -   | 5   | V                  |
| $T_A$             | Ambient temperature (Note 1) | -40 | -   | 85  | $^{\circ}\text{C}$ |

Note:

- (1)  $T_A$  represents the ambient temperature at which the circuit operates.
- (2) Operation beyond the recommended conditions for a long time may affect its reliability.

### 7.17.2 Electrical characteristic

$T_A=25^{\circ}\text{C}$ ,  $V_{\text{SUP1}}=V_{\text{SUP2}}=V_{\text{SUP}}=24\text{V}$ , the ground capacitance of GND=0  $V_{\text{SUP}}$  and the ground resistance of 5V are both  $1\mu\text{F}$ , and unless otherwise specified, all pins take GND as the reference point.

Table 66 Supply Voltage Parameters

| Symbol              | Parameter                                          | Min | Typ | Max | Unit |
|---------------------|----------------------------------------------------|-----|-----|-----|------|
| $V_{\text{SUPHY+}}$ | $V_{\text{SUP}}$ undervoltage high-level potential | 3.8 | 4.0 | 4.4 | V    |
| $V_{\text{SUPHY-}}$ | $V_{\text{SUP}}$ undervoltage low-level potential  | 3.6 | 3.8 | 4.2 | V    |
| $V_{\text{SUPHY}}$  | $V_{\text{SUP}}$ undervoltage hysteresis level     | 0.1 | 0.2 | 0.4 | V    |

Table 67 Supply Current Parameters

| Symbol            | Parameter                          | Condition                         | Min | Typ | Max  | Unit          |
|-------------------|------------------------------------|-----------------------------------|-----|-----|------|---------------|
| $I_{\text{SUPQ}}$ | $V_{\text{SUP}}$ quiescent current | $V_{\text{HIN}}=V_{\text{LIN}}=0$ | 500 | 650 | 1000 | $\mu\text{A}$ |
| $I_{\text{SUPD}}$ | $V_{\text{SUP}}$ dynamic current   | $f_{\text{VIN}}=20\text{kHz}$     | 0.8 | 2.0 | 3.5  | mA            |

Table 68 Time Parameters

| Symbol               | Parameter                             | Condition                                           | Min | Typ | Max | Unit |
|----------------------|---------------------------------------|-----------------------------------------------------|-----|-----|-----|------|
| $T_{\text{ON}}$      | Output rising edge transmission time  | No Load                                             | 170 | 230 | 400 | ns   |
| $T_{\text{OFF}}$     | Output falling edge transmission time | No Load                                             | 110 | 150 | 300 | ns   |
| $T_{\text{rise\_H}}$ | Output rise time of HO                | $C_L=1\text{nF}$                                    | 30  | 60  | 100 | ns   |
| $T_{\text{fall\_H}}$ | Output fall time of HO                | $C_L=1\text{nF}$                                    | 200 | 270 | 350 | ns   |
| $T_{\text{rise\_L}}$ | Output rise time of LO                | $C_L=1\text{nF}$                                    | 250 | 340 | 420 | ns   |
| $T_{\text{fall\_L}}$ | Output fall time of LO                | $C_L=1\text{nF}$                                    | 55  | 85  | 110 | ns   |
| DT                   | Dead time                             | No Load                                             | 250 | 400 | 600 | ns   |
| MT                   | High and low-side matching time       | $\Delta T_{\text{ON}} \ \& \ \Delta T_{\text{OFF}}$ | -   | -   | 100 | ns   |

**Table 69 Input-end Parameters**

| Symbol    | Parameter                  | Condition                 | Min | Typ | Max | Unit    |
|-----------|----------------------------|---------------------------|-----|-----|-----|---------|
| $I_{IN+}$ | Input high-level current   | $V_{HIN}$ or $V_{LIN}=5V$ | 15  | 25  | 35  | $\mu A$ |
| $I_{IN-}$ | Input low-level current    | $V_{HIN}$ or $V_{LIN}=0$  | -1  | 0   | 1   | $\mu A$ |
| $V_{IN+}$ | Input high-level potential | -                         | 1.7 | 2.1 | 2.6 | V       |
| $V_{IN-}$ | Input low-level potential  | -                         | 0.7 | 1.0 | 1.3 | V       |
| $V_{INH}$ | Input hysteresis level     | -                         | 0.7 | 1.1 | 1.5 | V       |

**Table 70 Output-end Parameters**

| Symbol    | Parameter         | Condition                                                | Min          | Typ          | Max         | Unit |
|-----------|-------------------|----------------------------------------------------------|--------------|--------------|-------------|------|
| $I_{HO+}$ | HO output current | $V_{HIN}=0$ , $V_{HO}=V_{SUP}$ , $PWD \leq 10\mu s$      | 200          | 260          | 350         | mA   |
| $I_{HO-}$ | HO sink current   | $V_{HIN}=5V$ , $V_{HO}=V_{SUP}-11V$ , $PWD \leq 10\mu s$ | 65           | 80           | 95          | mA   |
| $I_{LO+}$ | LO output current | $V_{LIN}=5V$ , $V_{LO}=0$ , $PWD \leq 10\mu s$           | 35           | 50           | 65          | mA   |
| $I_{LO-}$ | LO sink current   | $V_{LIN}=0$ , $V_{LO}=11V$ , $PWD \leq 10\mu s$          | 200          | 240          | 280         | mA   |
| $V_{HO}$  | HO output voltage | $V_{LIN}=0V$ , $V_{HIN}=5V$                              | $V_{SUP}-13$ | $V_{SUP}-11$ | $V_{SUP}-9$ | V    |
| $V_{LO}$  | LO output voltage | $V_{LIN}=5V$ , $V_{HN}=0V$                               | 9            | 11           | 13          | V    |

**Table 71 LDO Parameters**

| Symbol          | Parameter                        | Condition                               | Min | Typ | Max | Unit     |
|-----------------|----------------------------------|-----------------------------------------|-----|-----|-----|----------|
| $V_{5V}$        | Output voltage range             | $V_{SUP}=5.5V \sim 30V$                 | 4.8 | 5.0 | 5.2 | V        |
| $I_{load}$      | Output current range             | $V_{SUP}=5.5V \sim 30V$                 | -   | -   | 60  | mA       |
| $\Delta V_O$    | Voltage regulation rate          | $I_{load}=60mA$ , $V_{SUP}=6V \sim 30V$ | -   | 5   | 30  | mV       |
| $\Delta V_{OL}$ | Load regulation rate             | $V_{SUP}=24V$ , $I_{load}=0 \sim 60mA$  | -   | 15  | 50  | mV       |
| $I_{limit}$     | Short circuit protection current | -                                       | -   | 10  | 20  | mA       |
| $C_L$           | Load capacitance                 | -                                       | 2.2 | 4.7 | 100 | $\mu F$  |
| ESR             | Equivalent series resistance     | -                                       | 0   | 0   | 1   | $\Omega$ |

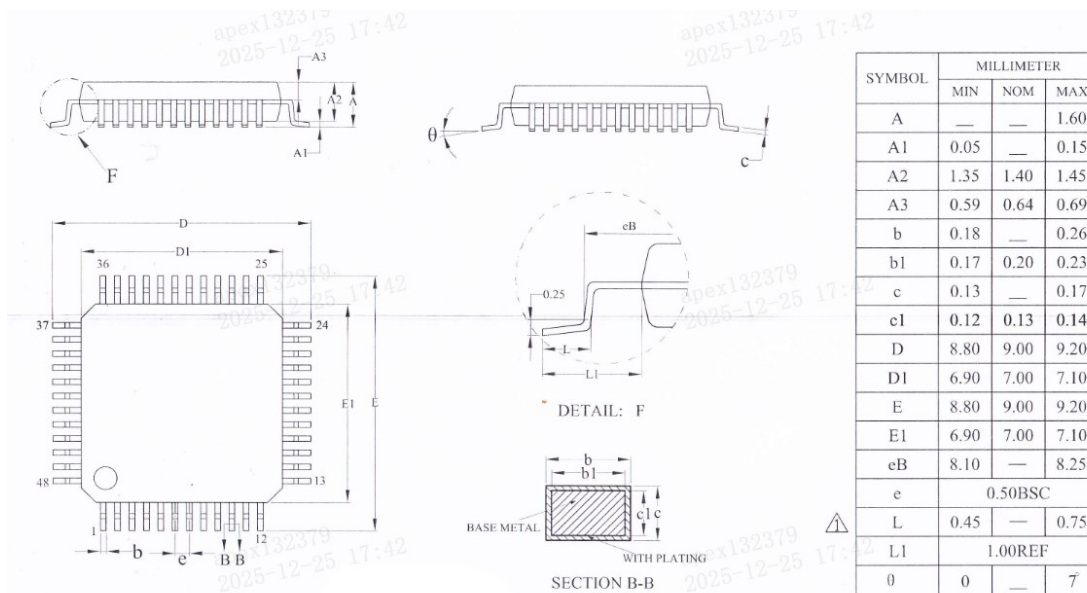
**Table 72 Over-temperature Protection**

| Symbol      | Parameter                                 | Condition | Min | Typ | Max | Unit        |
|-------------|-------------------------------------------|-----------|-----|-----|-----|-------------|
| $OTP_{HY+}$ | High value of over-temperature protection | -         | 150 | 160 | 170 | $^{\circ}C$ |
| $OTP_{HY-}$ | Low value of over-temperature protection  | -         | 125 | 135 | 145 | $^{\circ}C$ |
| $OTP_{HY}$  | Over-temperature protection hysteresis    | -         | 10  | 25  | 35  | $^{\circ}C$ |

## 8 Package Information

### 8.1 LQFP48 Package Information

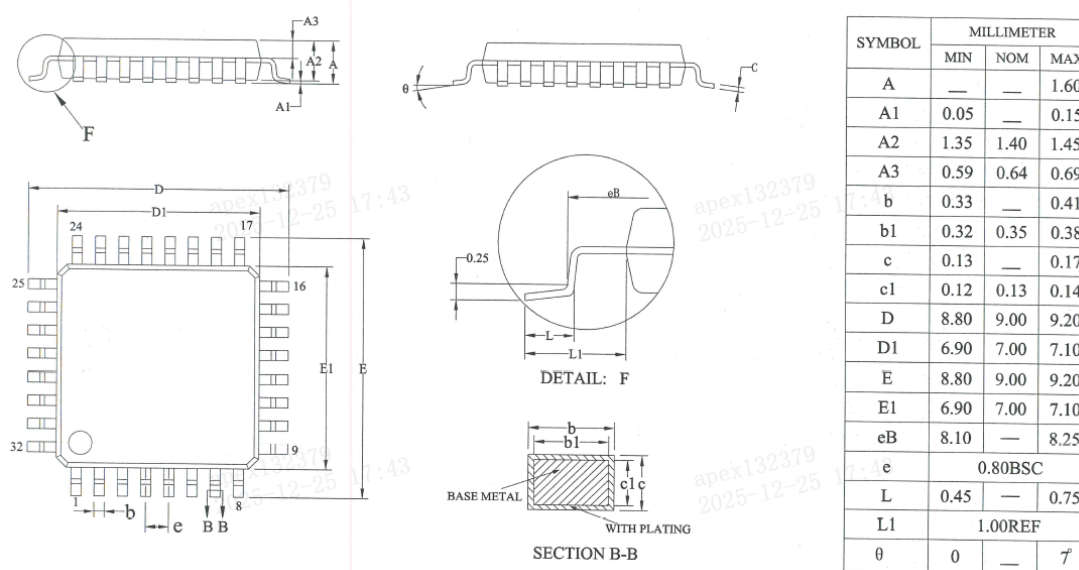
Figure 28 LQFP48 Package Diagram



Note: The figure is not drawn to scale.

### 8.2 LQFP32 Package Information

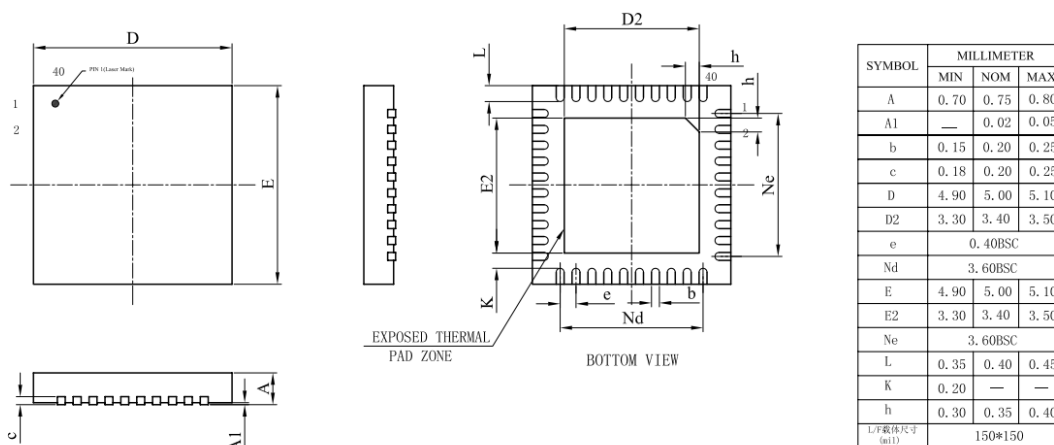
Figure 29 LQFP32 Package Diagram



Note: The figure is not drawn to scale.

## 8.3 QFN40 Package Information

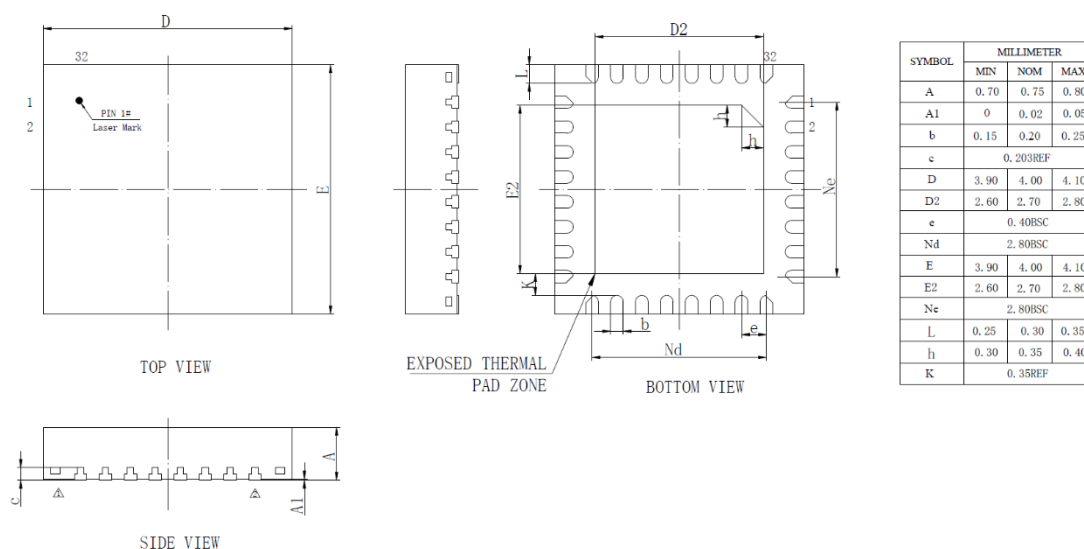
Figure 30 QFN40 Package Diagram



Note: The figure is not drawn to scale.

## 8.4 QFN32 Package Information

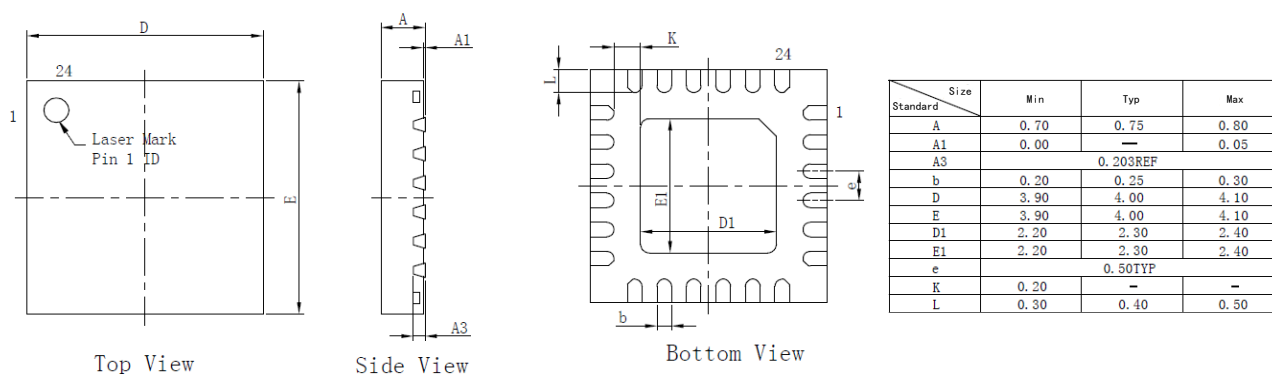
Figure 31 QFN32 Package Diagram



Note: The figure is not drawn to scale.

## 8.5 QFN24 Package Information

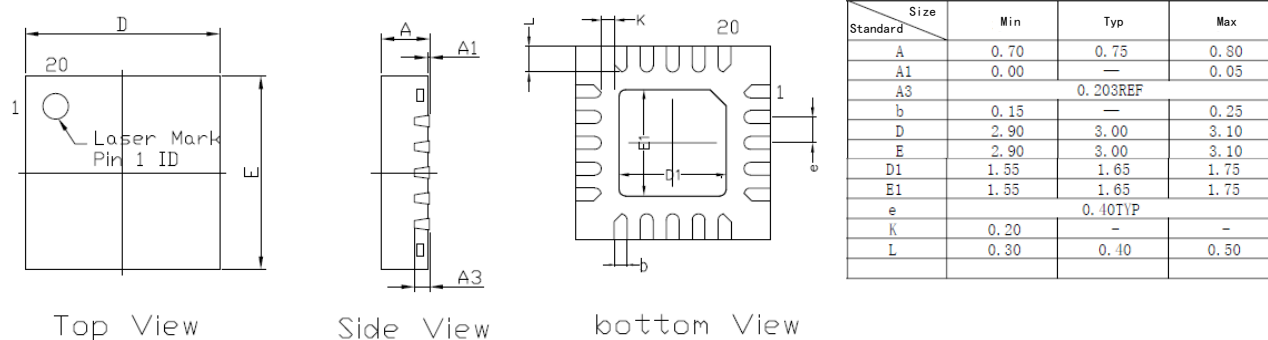
Figure 32 QFN24 Package Diagram



Note: The figure is not drawn to scale.

## 8.6 QFN20 Package Information

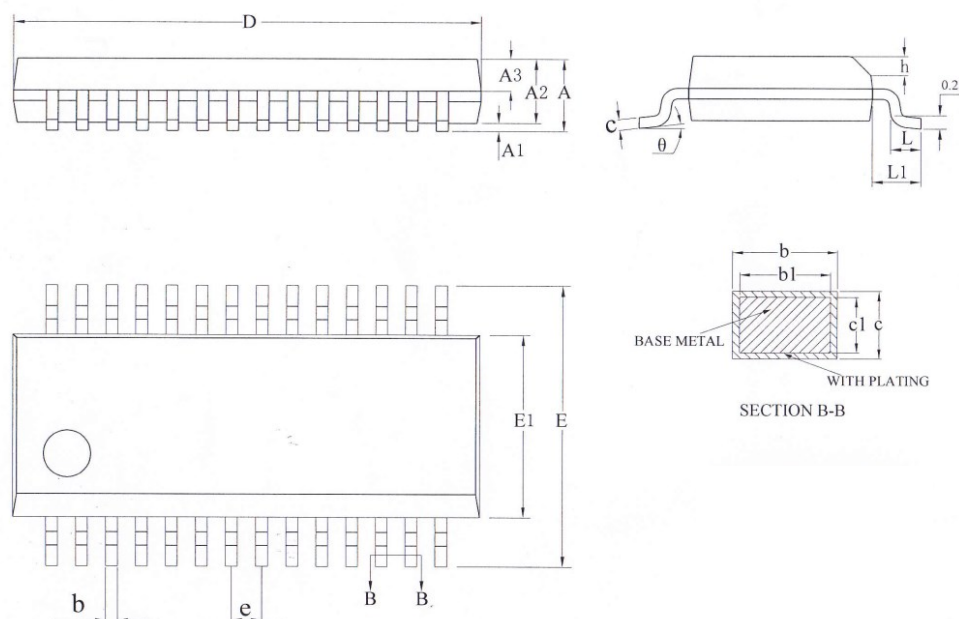
Figure 33 QFN20 Package Diagram



Note: The figure is not drawn to scale.

## 8.7 SSOP28 Package Information

Figure 34 SSOP28 Package Diagram

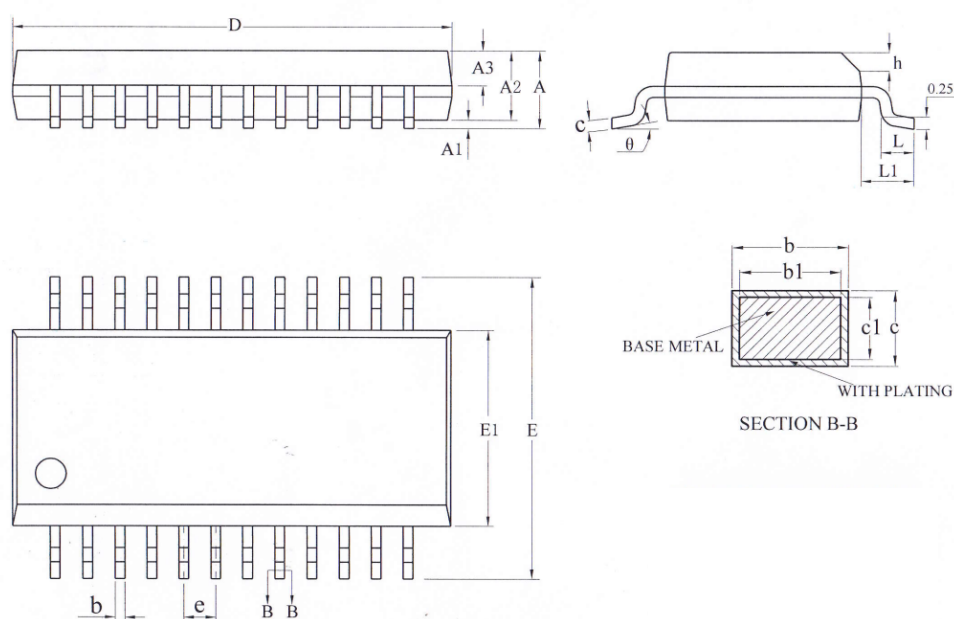


| SYMBOL | MILLIMETER |      |       |
|--------|------------|------|-------|
|        | MIN        | NOM  | MAX   |
| A      | —          | —    | 1.75  |
| A1     | 0.05       | —    | 0.225 |
| A2     | 1.30       | 1.40 | 1.50  |
| A3     | 0.60       | 0.65 | 0.70  |
| b      | 0.23       | —    | 0.31  |
| b1     | 0.22       | 0.25 | 0.28  |
| c      | 0.20       | —    | 0.24  |
| c1     | 0.19       | 0.20 | 0.21  |
| D      | 9.80       | 9.90 | 10.00 |
| E      | 5.80       | 6.00 | 6.20  |
| E1     | 3.80       | 3.90 | 4.00  |
| e      | 0.635BSC   |      |       |
| h      | 0.25       | —    | 0.50  |
| L      | 0.50       | —    | 0.80  |
| L1     | 1.05BSC    |      |       |
| θ      | 0°         | —    | 8°    |

Note: The figure is not drawn to scale.

## 8.8 SSOP24 Package Information

Figure 35 SSOP24 Package Diagram



| SYMBOL | MILLIMETER |      |      |
|--------|------------|------|------|
|        | MIN        | NOM  | MAX  |
| A      | —          | —    | 1.75 |
| A1     | 0.10       | 0.15 | 0.25 |
| A2     | 1.30       | 1.40 | 1.50 |
| A3     | 0.60       | 0.65 | 0.70 |
| b      | 0.23       | —    | 0.31 |
| b1     | 0.22       | 0.25 | 0.28 |
| c      | 0.20       | —    | 0.24 |
| c1     | 0.19       | 0.20 | 0.21 |
| D      | 8.55       | 8.65 | 8.75 |
| E      | 5.80       | 6.00 | 6.20 |
| E1     | 3.80       | 3.90 | 4.00 |
| e      | 0.635BSC   |      |      |
| h      | 0.30       | —    | 0.50 |
| L      | 0.50       | —    | 0.80 |
| L1     | 1.05REF    |      |      |
| θ      | 0          | —    | 8°   |

Note: The figure is not drawn to scale.

## 8.9 Package Designator

Figure 36 LQFP Package Designator

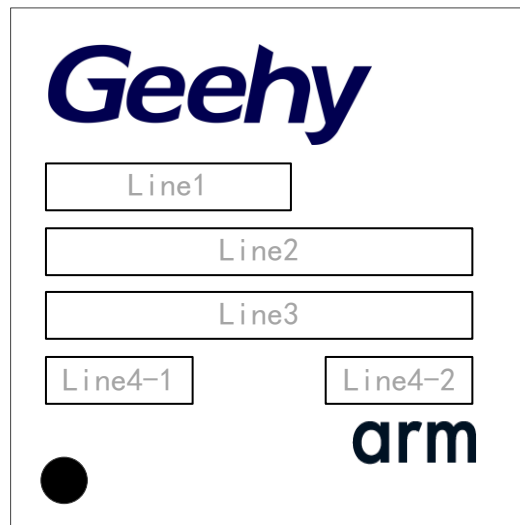


Table 73 LQFP silk-screen printing figure description

| Symbols and Icons | description                      |
|-------------------|----------------------------------|
| <b>Geehy</b>      | Geehy                            |
| Line1             | Product Series                   |
| Line2             | product model                    |
| Line3             | batch number                     |
| Line4-1           | Internal traceability code       |
| Line4-2           | Year and week number             |
| <b>arm</b>        | Arm authorization identification |
| ●                 | PIN1 location                    |

Note: The number of digits in each column above is not fixed.

Figure 37 QFN Package Designator

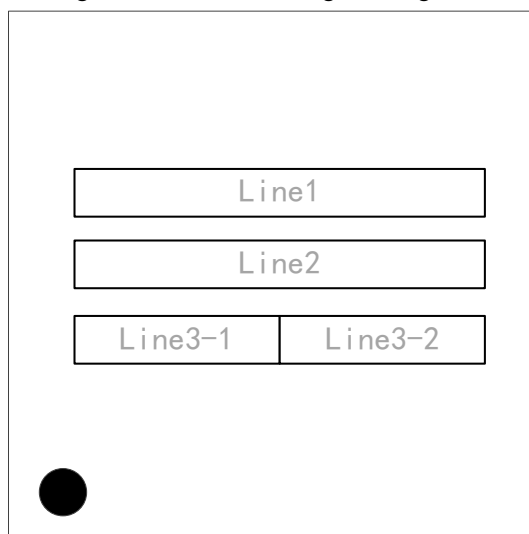


Table 74 QFN silk-screen printing figure description

| Symbols and Icons                                                                   | description                |
|-------------------------------------------------------------------------------------|----------------------------|
| Line1                                                                               | product model              |
| Line2                                                                               | batch number               |
| Line3-1                                                                             | Internal traceability code |
| Line3-2                                                                             | Year and week number       |
|  | PIN1 location              |

Note: The number of digits in each column above is not fixed.

Figure 38 SSOP Package Designator

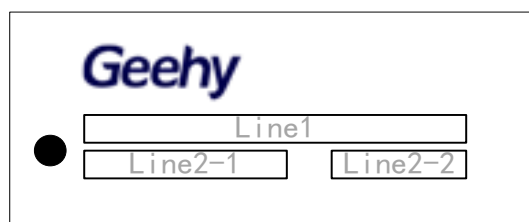


Table 75 SSOP silk-screen printing figure description

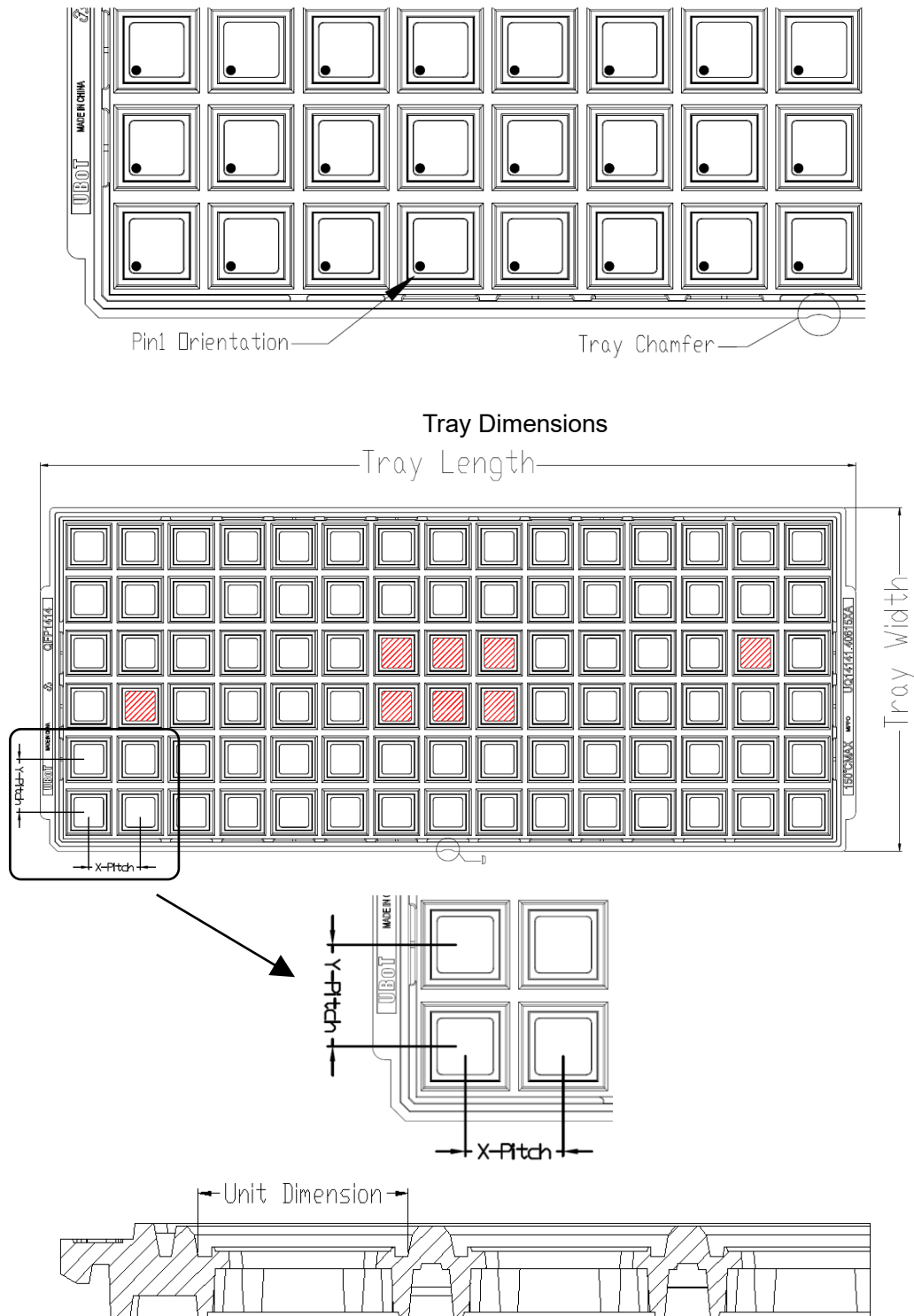
| Symbols and Icons                                                                   | description          |
|-------------------------------------------------------------------------------------|----------------------|
|  | Geehy                |
| Line1                                                                               | product model        |
| Line2-1                                                                             | batch number         |
| Line2-2                                                                             | Year and week number |
|  | PIN1 location        |

Note: The number of digits in each column above is not fixed.

## 9 Packaging Information

### 9.1 Tray packaging

Figure 39 Tray Packaging Diagram



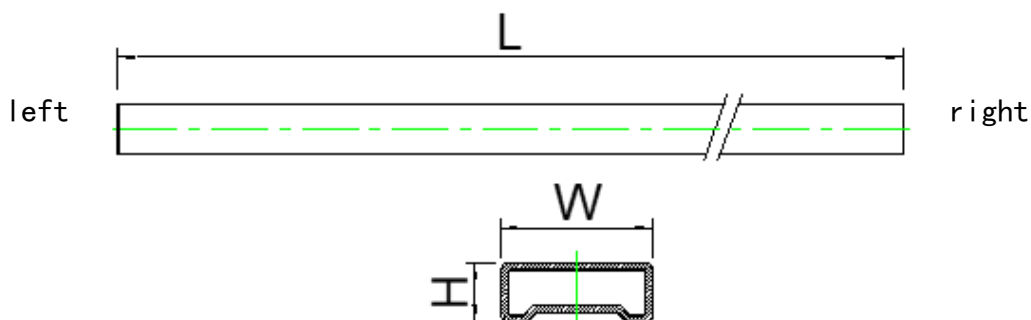
Note: All photos are for reference only, and the appearance is subject to the product.

Table 76 Parameter Specification Table of Pallet Packaging

| Device       | Package Type | Pins | SPQ  | X-Dimension (mm) | Y-Dimension (mm) | X-Pitch (mm) | Y-Pitch (mm) | Tray Length (mm) | Tray Width (mm) |
|--------------|--------------|------|------|------------------|------------------|--------------|--------------|------------------|-----------------|
| G32F031K8T6  | LQFP         | 32   | 2500 | 9.7              | 9.7              | 12.2         | 12.6         | 322.6            | 135.9           |
| G32F031K8U6  | QFN          | 32   | 4900 | 4.185            | 4.185            | 8.8          | 9.2          | 322.6            | 135.9           |
| G32F031E8U6  | QFN          | 24   | 4900 | 4.2              | 4.2              | 8.8          | 9.2          | 322.6            | 135.9           |
| G32F031F8U6  | QFN          | 20   | 6240 | 3.2              | 3.2              | 7.5          | 7.5          | 322.6            | 135.9           |
| G32F031K8T7  | LQFP         | 32   | 2500 | 9.7              | 9.7              | 12.2         | 12.6         | 322.6            | 135.9           |
| G32F031K8U7  | QFN          | 32   | 4900 | 4.185            | 4.185            | 8.8          | 9.2          | 322.6            | 135.9           |
| G32F031E8U7  | QFN          | 24   | 4900 | 4.2              | 4.2              | 8.8          | 9.2          | 322.6            | 135.9           |
| G32F031F8U7  | QFN          | 20   | 6240 | 3.2              | 3.2              | 7.5          | 7.5          | 322.6            | 135.9           |
| G32M3114C8T6 | LQFP         | 48   | 2500 | 9.7              | 9.7              | 12.2         | 12.6         | 322.6            | 135.9           |
| G32M3114H8U6 | QFN          | 40   | 4900 | 5.2              | 5.2              | 8.7          | 9.0          | 322.6            | 135.9           |
| G32M3115H8U6 | QFN          | 40   | 4900 | 5.2              | 5.2              | 8.7          | 9.0          | 322.6            | 135.9           |
| G32M3122K8T6 | LQFP         | 32   | 2500 | 9.7              | 9.7              | 12.2         | 12.6         | 322.6            | 135.9           |
| G32M3114C8T7 | LQFP         | 48   | 2500 | 9.7              | 9.7              | 12.2         | 12.6         | 322.6            | 135.9           |
| G32M3114H8U7 | QFN          | 40   | 4900 | 5.2              | 5.2              | 8.7          | 9.0          | 322.6            | 135.9           |
| G32M3115H8U7 | QFN          | 40   | 4900 | 5.2              | 5.2              | 8.7          | 9.0          | 322.6            | 135.9           |
| G32M3122K8T7 | LQFP         | 32   | 2500 | 9.7              | 9.7              | 12.2         | 12.6         | 322.6            | 135.9           |

## 9.2 Tube packaging

Figure 40 Tube package drawing



Note: All photos are for reference only, and the appearance is subject to the product.

Table 77 Specification table of tube packaging parameters

| Device       | Package Type | Pins | SPQ  | L(mm) | W(mm) | H(mm) |
|--------------|--------------|------|------|-------|-------|-------|
| G32F031G8S6  | SSOP         | 28   | 5000 | 520   | 7.8   | 3.4   |
| G32F031E8S6  | SSOP         | 24   | 5000 | 520   | 7.8   | 3.4   |
| G32M3122G8S6 | SSOP         | 28   | 5000 | 520   | 7.8   | 3.4   |
| G32M3122E8S6 | SSOP         | 24   | 5000 | 520   | 7.8   | 3.4   |

Note: SPQ= Smallest Package Quantity.

## 10 Ordering Information

Table 78 Product naming definition for F031

| product name |                       |       |                             |
|--------------|-----------------------|-------|-----------------------------|
| G32F031K8T6  |                       |       |                             |
| Name Example | Definition            | Name  | Information                 |
| G32          | Product Series        | G32   | Arm -based 32-bit MCU       |
| F            | Product type          | F     | Electrical machinery        |
| 031          | Product subseries     | 031   | General                     |
| G            | Number of pins        | F     | 20 pins                     |
|              |                       | E     | 24 pins                     |
|              |                       | G     | 28 pins                     |
|              |                       | K     | 32 pins                     |
| 8            | Flash memory capacity | 8     | 64KB                        |
| T            | Package               | T     | LQFP                        |
|              |                       | U     | QFN                         |
|              |                       | S     | SSOP                        |
| 6            | Temperature range     | 6     | temperature range:-40℃~85℃  |
|              |                       | 7     | temperature range:-40℃~105℃ |
| T            | pack                  | Blank | Tray packaging              |
|              |                       | T     | Tube packaging              |

Table 79 Product naming definition for M3122/M3114/M3115

| product name |                          |      |                       |
|--------------|--------------------------|------|-----------------------|
| G32M3114C8T6 |                          |      |                       |
| Name Example | Definition               | Name | Information           |
| G32          | Product Series           | G32  | Arm -based 32-bit SoC |
| M            | Product type             | M    | 电机控制型                 |
| 31           | Product type             | 31   | 031                   |
| 1            | Driver type              | 1    | NN Sip                |
|              |                          | 2    | PN Sip                |
| 4            | Driver voltage endurance | 2    | 40V                   |
|              |                          | 4    | 200V/1A               |
|              |                          | 5    | 200V/2A               |
| K            | Number of pins           | E    | 24 pins               |
|              |                          | G    | 28 pins               |
|              |                          | K    | 32 pins               |
|              |                          | H    | 40 pins               |
|              |                          | C    | 48 pins               |
| 8            | Flash memory capacity    | 8    | 64KB                  |

| product name |                   |       |                             |
|--------------|-------------------|-------|-----------------------------|
| T            | Package           | T     | LQFP                        |
|              |                   | U     | QFN                         |
|              |                   | S     | SSOP                        |
| 6            | Temperature range | 6     | temperature range:-40℃~85℃  |
|              |                   | 7     | temperature range:-40℃~105℃ |
| T            | pack              | Blank | Tray packaging              |
|              |                   | T     | Tube packaging              |

Table 80 Ordering Information List

| Order Code     | FLASH (KB) | SRAM (KB) | Package | SPQ  | Temperature range |
|----------------|------------|-----------|---------|------|-------------------|
| G32F031K8T6    | 64         | 8         | LQFP32  | 2500 | -40℃~85℃          |
| G32F031K8U6    | 64         | 8         | QFN32   | 4900 | -40℃~85℃          |
| G32F031E8U6    | 64         | 8         | QFN24   | 4900 | -40℃~85℃          |
| G32F031F8U6    | 64         | 8         | QFN20   | 6240 | -40℃~85℃          |
| G32F031G8S6-T  | 64         | 8         | SSOP28  | 5000 | -40℃~85℃          |
| G32F031E8S6-T  | 64         | 8         | SSOP24  | 5000 | -40℃~85℃          |
| G32F031K8T7    | 64         | 8         | LQFP32  | 2500 | -40℃~105℃         |
| G32F031K8U7    | 64         | 8         | QFN32   | 4900 | -40℃~105℃         |
| G32F031E8U7    | 64         | 8         | QFN24   | 4900 | -40℃~105℃         |
| G32F031F8U7    | 64         | 8         | QFN20   | 6240 | -40℃~105℃         |
| G32M3114C8T6   | 64         | 8         | LQFP48  | 2500 | -40℃~85℃          |
| G32M3114H8U6   | 64         | 8         | QFN40   | 4900 | -40℃~85℃          |
| G32M3115H8U6   | 64         | 8         | QFN40   | 4900 | -40℃~85℃          |
| G32M3122K8T6   | 64         | 8         | LQFP32  | 2500 | -40℃~85℃          |
| G32M3122G8S6-T | 64         | 8         | SSOP28  | 5000 | -40℃~85℃          |
| G32M3122E8S6-T | 64         | 8         | SSOP24  | 5000 | -40℃~85℃          |
| G32M3114C8T7   | 64         | 8         | LQFP48  | 2500 | -40℃~105℃         |
| G32M3114H8U7   | 64         | 8         | QFN40   | 4900 | -40℃~105℃         |
| G32M3115H8U7   | 64         | 8         | QFN40   | 4900 | -40℃~105℃         |
| G32M3122K8T7   | 64         | 8         | LQFP32  | 2500 | -40℃~105℃         |

## 11 Commonly Used Function Module Denomination

Table 81 Commonly Used Function Module Denomination

| Full name                                                   | Abbreviation |
|-------------------------------------------------------------|--------------|
| Reset management unit                                       | RMU          |
| Clock management unit                                       | CMU          |
| Reset and clock management                                  | RCC          |
| External Interrupt                                          | EINT         |
| General-purpose IO                                          | GPIO         |
| Multiplexing IO                                             | AFIO         |
| Wake-up controller                                          | WUPT         |
| Buzzer                                                      | BUZZER       |
| Independent watchdog timer                                  | IWDG         |
| Window watchdog timer                                       | WWDG         |
| Timer                                                       | TMR          |
| CRC Controller                                              | CRC          |
| Power management unit                                       | PMU          |
| DMA controller                                              | DMA          |
| Analog-to-digital converter                                 | ADC          |
| Real-time Clock                                             | RTC          |
| External memory controller                                  | EMMC         |
| Controller Area Network                                     | CAN          |
| I2C Interface                                               | I2C          |
| Serial Peripheral Interface                                 | SPI          |
| Universal asynchronous receiver transmitter                 | UART         |
| Universal synchronous and asynchronous receiver transmitter | USART        |
| Flash interface control unit                                | FMC          |
| Safe digital input/output                                   | SDIO         |
| Digital camera interface                                    | DCI          |

## 12 Revision

Table 82 Document Revision History

| Date            | Version | Change History                                                                                                                                                                                                      |
|-----------------|---------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| September, 2025 | 1.0     | <ul style="list-style-type: none"> <li>Initial version</li> </ul>                                                                                                                                                   |
| May, 2026       | 1.1     | <ul style="list-style-type: none"> <li>Add the sealing model information</li> </ul>                                                                                                                                 |
| May, 2026       | 1.2     | <ul style="list-style-type: none"> <li>Modify the M3115 pin diagram and pin definitions</li> </ul>                                                                                                                  |
| July, 2026      | 1.3     | <ul style="list-style-type: none"> <li>Modify the electrical characteristics and levitation offset voltage of M3115</li> <li>Modify the pre-division coefficient in "Table 22 IWDT and WWDT Comparison "</li> </ul> |

# Statement

This document is formulated and published by Geehy Semiconductor Co., Ltd. (hereinafter referred to as "Geehy"). The contents in this document are protected by laws and regulations of trademark, copyright and software copyright. Geehy reserves the right to make corrections and modifications to this document at any time. Read this document carefully before using Geehy products. Once you use the Geehy product, it means that you (hereinafter referred to as the "users") have known and accepted all the contents of this document. Users shall use the Geehy product in accordance with relevant laws and regulations and the requirements of this document.

## 1. Ownership

This document can only be used in connection with the corresponding chip products or software products provided by Geehy. Without the prior permission of Geehy, no unit or individual may copy, transcribe, modify, edit or disseminate all or part of the contents of this document for any reason or in any form.

The “极海” or “Geehy” words or graphics with “®” or “™” in this document are trademarks of Geehy. Other product or service names displayed on Geehy products are the property of their respective owners.

## 2. No Intellectual Property License

Geehy owns all rights, ownership and intellectual property rights involved in this document.

Geehy shall not be deemed to grant the license or right of any intellectual property to users explicitly or implicitly due to the sale or distribution of Geehy products or this document.

If any third party's products, services or intellectual property are involved in this document, it shall not be deemed that Geehy authorizes users to use the aforesaid third party's products, services or intellectual property. Any information regarding the application of the product, Geehy hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party, unless otherwise agreed in sales order or sales contract.

## 3. Version Update

Users can obtain the latest document of the corresponding models when ordering Geehy products.

If the contents in this document are inconsistent with Geehy products, the agreement in the sales order or the sales contract shall prevail.

## 4. Information Reliability

The relevant data in this document are obtained from batch test by Geehy Laboratory or cooperative third-party testing organization. However, clerical errors in correction or errors caused by differences in testing environment may occur inevitably. Therefore, users should understand that Geehy does not bear any responsibility for such errors that may occur in this document. The relevant data in this document are only used to guide users as performance parameter reference and do not constitute Geehy's guarantee for any product performance.

Users shall select appropriate Geehy products according to their own needs, and effectively verify and test the applicability of Geehy products to confirm that Geehy products meet their own needs, corresponding standards, safety or other reliability requirements. If losses are caused to users due to user's failure to fully verify and test Geehy products, Geehy will not bear any responsibility.

## 5. Legality

USERS SHALL ABIDE BY ALL APPLICABLE LOCAL LAWS AND REGULATIONS WHEN USING THIS DOCUMENT AND THE MATCHING GEEHY PRODUCTS. USERS SHALL UNDERSTAND THAT THE PRODUCTS MAY BE RESTRICTED BY THE EXPORT, RE-EXPORT OR OTHER LAWS OF THE COUNTRIES OF THE PRODUCTS SUPPLIERS, GEEHY, GEEHY DISTRIBUTORS AND USERS. USERS (ON BEHALF OR ITSELF, SUBSIDIARIES AND AFFILIATED ENTERPRISES) SHALL AGREE AND PROMISE TO ABIDE BY ALL APPLICABLE LAWS AND REGULATIONS ON THE EXPORT AND RE-EXPORT OF GEEHY PRODUCTS AND/OR TECHNOLOGIES AND DIRECT PRODUCTS.

## 6. Disclaimer of Warranty

THIS DOCUMENT IS PROVIDED BY GEEHY "AS IS" AND THERE IS NO WARRANTY OF ANY KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, THE WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, TO THE EXTENT PERMITTED BY APPLICABLE LAW.

GEEHY'S PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED FOR USE AS CRITICAL COMPONENTS IN MILITARY, LIFE-SUPPORT, POLLUTION CONTROL, OR HAZARDOUS SUBSTANCES MANAGEMENT SYSTEMS, NOR WHERE FAILURE COULD RESULT IN INJURY, DEATH, PROPERTY OR ENVIRONMENTAL DAMAGE.

IF THE PRODUCT IS NOT LABELED AS "AUTOMOTIVE GRADE," IT SHOULD NOT BE CONSIDERED SUITABLE FOR AUTOMOTIVE APPLICATIONS. GEEHY ASSUMES NO LIABILITY FOR THE USE BEYOND ITS SPECIFICATIONS OR GUIDELINES.

THE USER SHOULD ENSURE THAT THE APPLICATION OF THE PRODUCTS COMPLIES WITH ALL RELEVANT STANDARDS, INCLUDING BUT NOT LIMITED TO SAFETY, INFORMATION SECURITY,

AND ENVIRONMENTAL REQUIREMENTS. THE USER ASSUMES FULL RESPONSIBILITY FOR THE SELECTION AND USE OF GEEHY PRODUCTS. GEEHY WILL BEAR NO RESPONSIBILITY FOR ANY DISPUTES ARISING FROM THE SUBSEQUENT DESIGN OR USE BY USERS.

#### 7. Limitation of Liability

IN NO EVENT, UNLESS REQUIRED BY APPLICABLE LAW OR AGREED TO IN WRITING WILL GEEHY OR ANY OTHER PARTY WHO PROVIDES THE DOCUMENT AND PRODUCTS "AS IS", BE LIABLE FOR DAMAGES, INCLUDING ANY GENERAL, SPECIAL, DIRECT, INCIDENTAL OR CONSEQUENTIAL DAMAGES ARISING OUT OF THE USE OR INABILITY TO USE THE DOCUMENT AND PRODUCTS (INCLUDING BUT NOT LIMITED TO LOSSES OF DATA OR DATA BEING RENDERED INACCURATE OR LOSSES SUSTAINED BY USERS OR THIRD PARTIES). THIS COVERS POTENTIAL DAMAGES TO PERSONAL SAFETY, PROPERTY, OR THE ENVIRONMENT, FOR WHICH GEEHY WILL NOT BE RESPONSIBLE.

#### 8. Scope of Application

The information in this document replaces the information provided in all previous versions of the document.

© 2026 Geehy Semiconductor Co., Ltd. - All Rights Reserved